Chapter 1
GaAs Field Effect Transistor

1.1 Introduction

In this chapter, an introduction to gallium arsenide is first presented followed by a description of the GaAs FET material (substrate, channel) and its manufacturing. We then present its operation principal and DC characteristics.

1.2 Crystalline structure of GaAs

GaAs is a compound semiconductor combining group III (Ga) and group V(As) element; while Ga is rare element produced as a by product in Al or Zn production; As is an abundant element which can be produced from Sulphure ores such as As_2S_4 and As_2S_3 . Schmidth; first created GaAs in 1920[11]; and found it to have the cubic Sphalerite (zinc blende) lattice. This has a face centers cubic (FCC) translation symmetry with a base of one GaAs molecule; one atom at 000 and the other at 111of the non primitive FCC unit cubic. (Figure1.1)

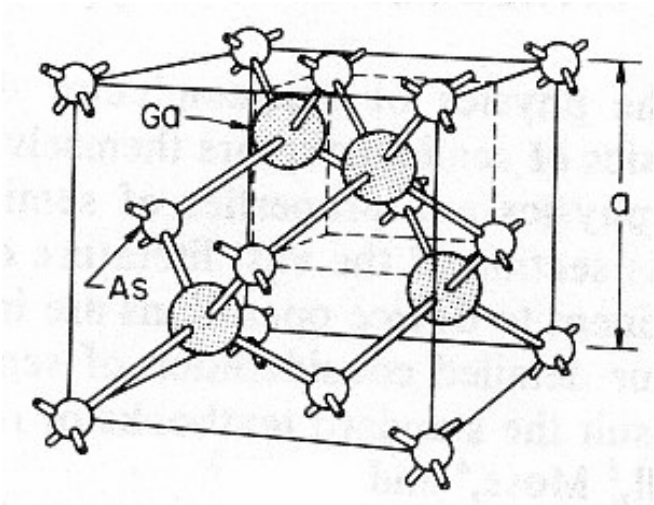

Fig 1.1: Illustration of unit cell of GaAs lattice which has a zinc blende structure

The lattice is formed by an overlap of two FCC lattices. One of Ga and the other of As; shifted one from the other by transition vector r=a(1/4,1/4,1/4); where a is the lattice constant. The banding between Ga and As is predominantly covalent.

1.3 Properties of GaAs

The wide band gap of gallium arsenide and the resulting decrease in the thermal electron hole production rate lead to a low intrinsic density of free carrier. So it is relatively easy to add dopants to compensate these carriers and produce semi insulating (SI) of GaAs. This property (SI) is very useful in isolating adjacent devices and withstand radiation damage. Its direct band gap gives it important optical properties. In addition band gap engineering –by alloying with other III and V elements– devices can be designed to emit and respond to a wide range of wave length susceptible to be exploited in optoelectronic industry.

Among of the most important advantage of GaAs is the ease and speed with which electron can move in it. Its electron mobility is about five times higher and the electron saturation velocity is about twice that of Si. This leads to the reduction of transit and switching times of devices.

One area of impact of GaAs devices is in the microwave technology. At the forefront of this development is the maturity of the GaAs Metal Semiconductor Field Effect Transistor (MESFET's).

In spite of these advantages; there are some difficulties in its technology that limit its use to niche applications. The hardly obtainable stochiometry between the constituents (Ga and As).and the complex crystal structure tend to create a higher density of defects which can strongly influence the performance of devices and integrated circuits made of GaAs. GaAs is far less abundant than Silicon and hence is much more expensive. The GaAs bulk properties also pose manufacturing difficulties. The material is more brittle and weaker than silicon leading to thicker wafers and difficult manipulation. Poor substrates may not only degrade device and circuit performance but can affect the yield and reproducibility.

1.4 Material preparation

1.4.1 Bulk growth of the substrate material

several techniques are used to manufacture the substrate material. The Liquid Encapsulated Czochralski (LEC) is the most popular. Under a high purity, a crucible consisting of boron-nitride contains the molten gallium-arsenide (GaAs). A pulling rod holds the crystal which is pulled up carefully while rotating. To make dislocations grow out of the crystal the radius increases slowly in the area of the shoulder.

The Vertical Gradient Freez (VGF)Technology is an other famous process. Uses high purity gallium and arsenic which are mixed in an enclosed quartz ampoule. The growth starts with a seed placed at the bottom of the crucible, and because the temperature gradient used in the VGF process is significantly lower than the Liquid-encapsulated Czochralski (LEC) this enables for grow crystals that have a relatively low dislocation density and high uniformity process system are avoided.

1.4.2 Material for the conducting channel

For the high purity GaAs film grown on the substrate. Two methods are usually used. The single crystal layers are formed by epitaxy and ion implantation. The first is presented here since the device under study has uniformly doped channel and this is a characteristic of epitaxial techniques. An example of epitaxial methods is the Vapor-Phase Epitaxy. Fig1.2 shows a schematic and representation of the growth chamber for this system. In the horizontal unit hydro-chlorate flows over gallium to form the volatile GaCl. This material is then swept downstream where it mixes with arsine. At the temperature used; the arsine decomposes in stages, losing an attached hydrogen at each step. The simplified reactions for the system can be represented as follows:

a/ $2HCl+2Ga \longrightarrow 2GaCl+H_2$

b/ $AsH_x(x=0.1.2.) + GaCl \longrightarrow GaAs_{sol}+As4+GaCl3+H_2$

$GaAs_{sol} + HCl$

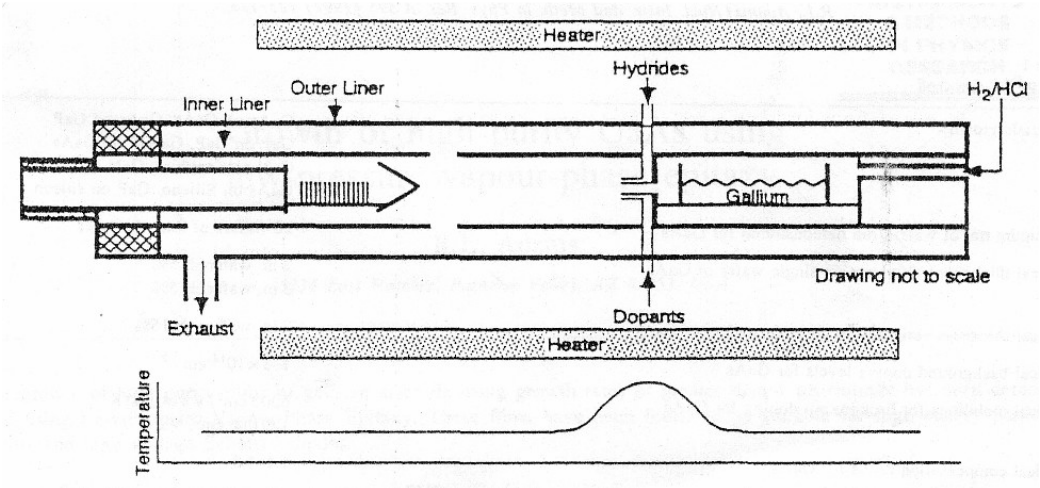

Fig 1.2: Illustration of vapor-phase epitaxy

1.5 The Metal Semiconductor Field Effect Transistor

1.5.1 General structure

Due to the basic conduction process which involves one kind of carrier (majority carriers), the FET is known as a unipolar transistor. The device consist of a high purity substrate of GaAs doped by Chromium (Cr) to make it semi insulating. An epitaxial layer is grown on the substrate, which is a very thin typically $0.1\mu m$ to $0.2\mu m$ thick. This layer is doped with silicon to form the conducting n-type channel. Carriers flow along this channel between two gold ohmic contacts; the drain and source, under an applied bias. To control the current flow; a gate which consist on a metallization of Aluminium, generally of rectangular form, posed between the drain and source over the channel. The gate and the epitaxial layer (channel) form a Schottky contact. At this contact there is a potential due to the difference of the work function of the metal and the electron affinity of the semiconductor.

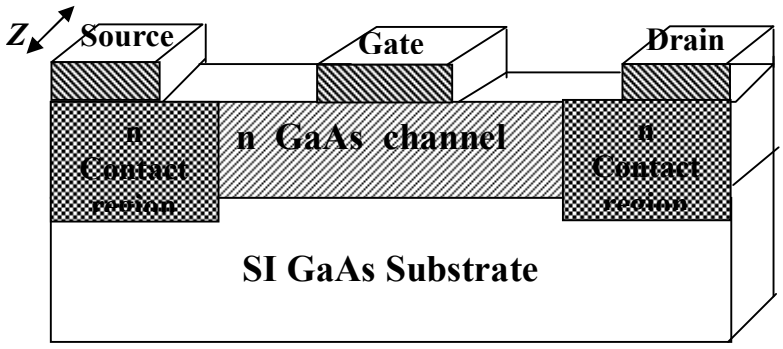

Fig 1.2: Illustration of typical MESFET structure

1.5.2 Principe of MESFET operation

If the source is connected to the ground, and the gate polarized negatively, an empty region of free electron is built under the gate and the conducting cross sectional area of the channel is reduced. If the drain is positively polarized, a current I_D circulates in the channel and the depletion region is wider at the drain side than the source side. This leads to the graduated variation of the conducting cross section area along the channel.

For small drain-source voltage; the relative variation of the conducting cross section of the channel is unimportant; the channel conductance stay practically constant and the device act as an ohmic resistor. This is the linear or ohmic regime. At high drain-source voltage; the electric field in the channel becomes higher and the current present a non linear behavior, and tends to saturation. The channel length of the order of 1µm; hence the voltage for saturation is

low since the longitudinal field reaches an important level. If this field reaches a critical value; the saturation is determined by the electron velocity.

1.5.3 DC Characteristics

The field effect transistor was first modeled by W. Shockley in early 1950's. The model is based of the following approximations:

- A gradual channel, the applied voltage varies linearly from the source to the drain.
- Constant electron mobility, independent of electric field.
- Uniform channel doping profile.
- Abrupt boundary conditions.

We shall suppose; also that the semiconductor is homogeneous; containing a neutral density N_D; the density of interface states is negligible; the depletion region acts like a perfect insulator (empty of carriers). A gradual channel proposed by Shockley [28] is illustrated in figure 1.3. Although the original model referred to Junction FETs, the operation of MESFET is identical. Since the pn junction is replaced by a Schottky junction

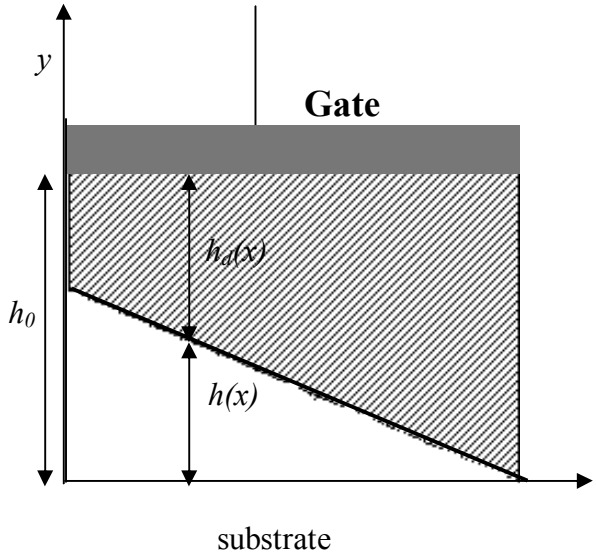

Fig 1.3: An illustration of the form of depletion region assumed under the gradual channel approximation. Reproduced from [27]

where $h_d(x), h(x)$ are the depths of the depleted and undepleted regions as function of position along the channel.

The incremental change of the channel potential dV can be expressed as :

$$dV = I_{ch} \cdot dR = I_{ch} \frac{dx}{q \cdot \mu_n \cdot N_D \cdot Z} \cdot \frac{1}{h(x)} \qquad 1.1$$

where $h(x) = h_0 - h_d(x)$ 1.2

h_0 represent the thickness of metallurgical channel (the full width of channel).

The potential varies slowly across the channel (gradual channel approximation). At each point; the thickness of depletion region can be determined from the solution of Poisson equation. The depletion layer width at a distance x from the source is given by the abrupt junction expression:

$$h_d(x)=\{2\cdot\varepsilon_s\cdot(V(x)-V_G+V_{Bi})/q\cdot N_D\}^{0.5} \quad 1.3$$

where V_{Bi} is the Schottky barrier built in voltage.

The electrical field within the channel perpendicular to the current is negligible compared to the field along the channel. The diffusion current component is neglected since the doping is uniform; and according to Ohm's law; the current density along the channel is taken at x-direction as :

$$J_x=\sigma\cdot E \quad 1.4$$

hence

$$J_x=-\sigma\cdot\left(\frac{\partial V}{\partial x}\right) \quad 1.5$$

where E is the electric field and σ is the conductivity defined as $\sigma=q\cdot N_D\cdot\mu_n$

μ_n represent the mobility which is assumed constant. When we suppose that no parallel current leakage exist, the channel current is given by

$$I_{ch}=-J_x\cdot Z\cdot h(x) \quad 1.6$$

Z is the width of the gate.

From equations (1. 3) and (1.6) the expression of current channel becomes:

$$I_{ch}=Z\cdot q\cdot N_D\cdot\mu_n\cdot\frac{dV}{dx}\left\{h_0-\sqrt{\frac{2\cdot\varepsilon(V(x)+V_{Bi}-V_G)}{q\cdot N_D}}\right\} \quad 1.7$$

or $$I_{ch}\,dx=Z\cdot q\cdot N_D\cdot\mu_n\cdot dV\left\{h_0-\sqrt{\frac{2\cdot\varepsilon(V(x)+V_{Bi}-V_G)}{q\cdot N_D}}\right\} \quad 1.8$$

integrating the left side of eq (1.8) with respect to x along the channel and the right side with respect to V and defining the pinch-off voltage V_p as the gate voltage needed to totally deplete the channel for zero V_{DS} given by [26]

$$V_p+V_{Bi}=\frac{q\cdot N_D\cdot}{2\cdot\varepsilon_s}h_0^2 \quad 1.9$$

we obtain the fundamental equation of field effect transistors

$$I_{ch}=G_0\left\{V_{DS}-\frac{2}{3}\frac{\left(V_{DS}+V_{Bi}-V_G\right)^{3/2}-\left(V_{Bi}-V_G\right)^{3/2}}{\left(V_{Bi}+V_p\right)^{1/2}}\right\} \quad 1.10$$

Note that the source is at the ground ($V=0$ at $x=0$) and ($V=V_D$ at $x=l$). In eq (1.10) G_0 is the conductance of the full open channel given by:

$$G_0=\frac{q\cdot\mu_n\cdot N_D\cdot Z\cdot h_0}{l} \quad 1.11$$

V_{DS} is the potential drop in the channel across the region directly under the gate. In the ohmic regime (the device operate in the linear region) V_{DS} is negligible compared to $V_{Bi}-V_G$ and using the Taylor expansion, taking V_{DS} as the perturbation, equation (1.10) then becomes:

$$I_{ch}=G_0\cdot V_{DS}\cdot\left\{1-\frac{\left(V_{Bi}-V_G\right)^{1/2}}{V_p^{1/2}}-\frac{V_{DS}}{4\cdot V_p^{1/2}\left(V_{Bi}-V_G\right)^{1/2}}\right\} \quad 1.12$$

we can simplify this equation further more to become

$$I_{ch}=G_0\cdot V_{DS}\cdot\left\{1-\sqrt{\frac{\left(V_{Bi}-V_G\right)}{\left(V_{Bi}-V_p\right)}}\right\} \quad 1.13$$

The active channel resistance is expressed from eq (1.13) using Ohm's law by :

$$R_c=R_{co}\left\{1-\left(\frac{V_{Bi}-V_G}{V_{Bi}-V_p}\right)^{0.5}\right\}^{-1} \quad 1.14$$

then $R_c=R_{co}\cdot K$ 1.15

where K is the channel opening factor; given as

$$K=\frac{1}{1-\sqrt{\frac{V_{Bi}-V_G}{V_{Bi}-V_p}}} \quad 1.16$$

and $R_{co}=\frac{1}{G_0}$ 1.17

R_{co} is the full open channel resistance .

Real devices have parasitic resistances associated with the ungated regions of the device; and resistance due to the non ideal contacts. The MESFET is accurately modeled using the following model .

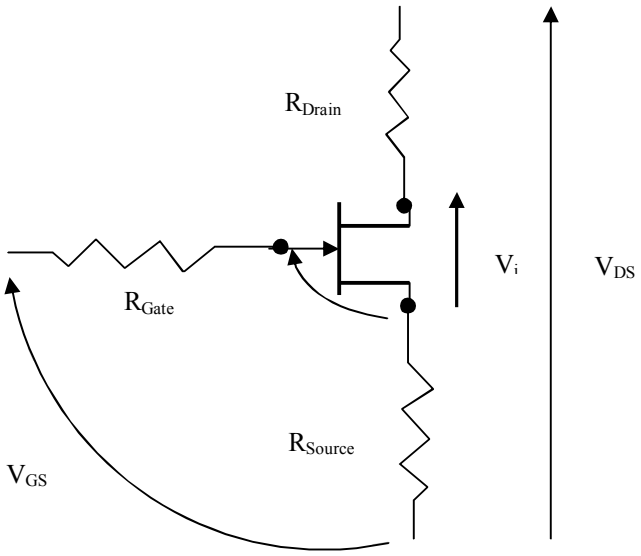

Fig 1.4: MESFET with parasitic resistances. Reproduced from [3]

The channel resistance which is $\frac{V_{DS}}{I_{ch}}$ is the combination of two resistances, is given by

$$R = R_s + R_c \qquad 1.18$$

R_S is the parasitic resistance.

we are of course assuming the absence of any significant resistance here, which must be added to full equations.

1.5.4 Saturation characteristics

For long devices (more than 1µm), the Shockley model reasonably describes the device characteristics. But for modern FETs with short gates, a significant discrepancies are encountered. One of the reason for this is believed to be the non-linear dependence of the drift velocity on the electric field at high fields because the mobility itself becomes electric field dependent[1]. However; there is no law which translates correctly this dependence. One of the analytical expressions usually used is;

$$\begin{cases} \mu_n = \mu_{no} \cdot \dfrac{1}{1 + \mu_{n0} \cdot \dfrac{|E|}{v_{ns}}} \\ \mu_p = \mu_{p0} \cdot \dfrac{1}{1 + \mu_{p0} \cdot \dfrac{|E|}{v_{ps}}} \end{cases} \qquad 1.19$$

The velocity-field characteristic tacking the mobility field dependence into account is shown in figure 1.5.

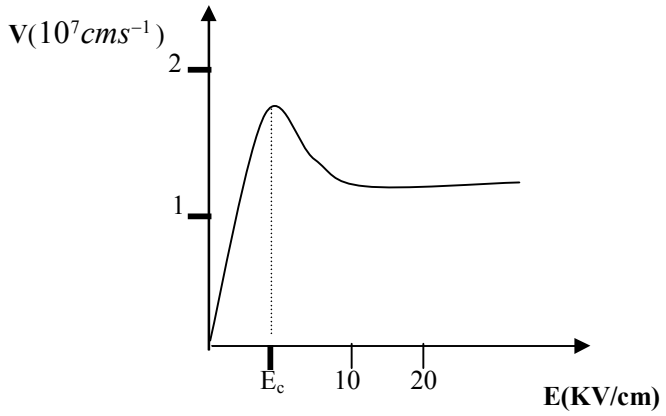

Fig 1.5: Electrons velocity as function of electric field.

At low fields (below a critical value) the velocity has a linear variation with the electrical field; followed by a saturation mechanism in velocity reaches it peak. The velocity-field curves are shown in Fig 1.6 .

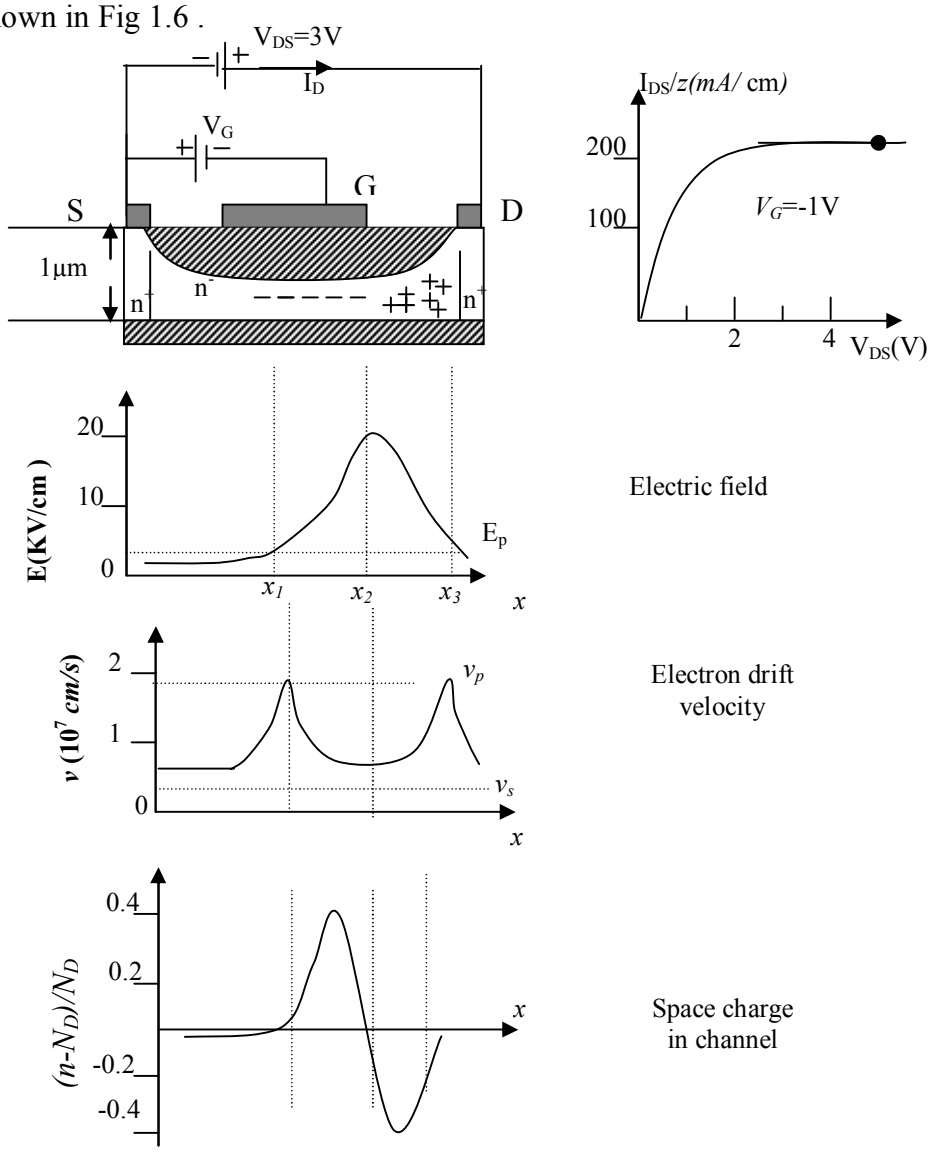

Fig 1.6: Channel cross section, electric field, drift velocity and space charge distribution in the channel of GaAs FET operated in the saturation region [34].

As the narrowest channel opening is near the drain end of the gate. the drift velocity reaches a peak at x_1 where the electric field E_c and then drops again as the electric field increases to reach the critical value E_{max} at x_2 . since the channel is narrowing and electrons are moving slower between x_1 and x_2 , heavy electron accumulation occurs to preserve a constant current. Exactly the opposite happens between x_2 and x_3. the channel widens and the electrons move faster causing a strong depletion layer.