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Elaboration, characterization and simulation of thin film transistors based on Zinc Oxide

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Abstract

The thesis explores the field of polycrystalline semiconductor oxides, particularly zinc oxide (ZnO), as a key component in thin-film transistors (TFTs) crucial for electronic applications like active-matrix liquid crystal displays (AMLCDs). Utilizing numerical simulations with SILVACO ATLAS, the study investigates four main areas. First, the temperature effect on pc-ZnO TFTs is examined, revealing a temperature-dependent drain current with activation energy varying linearly from 0.57 eV to 0.071 eV across different gate voltages. Second, the impact of illumination on PC-ZnO TFTs at a low temperature of 280 K is studied, manipulating electric mobility and deep defects. Third, the grain size and boundary effects on nano-crystalline zinc oxide TFTs are explored through experimental and numerical analysis, demonstrating the influence of deposition temperature on grain size and subsequent transfer characteristics. Lastly, TFTs made of ZnO thin films deposited on various substrates are investigated, detailing the deposition process, pressure control, and annealing conditions. The research provides valuable insights into optimizing the performance of ZnO-based TFTs for electronic applications.

Keywords: Elaboration, Characterization, Design, TFT, SILVACO ATLAS, Defects.

Résumé

La thèse explore le domaine des oxydes semi-conducteurs polycristallins, en particulier l'oxyde de zinc (ZnO), en tant que composant clé des transistors à couches minces (TFT) essentiels pour les applications électroniques telles que les écrans à cristaux liquides à matrice active (AMLCD). Utilisant des simulations numériques avec SILVACO ATLAS, l'étude examine quatre domaines principaux. Tout d'abord, l'effet de la température sur les TFT pc-ZnO est examiné, révélant un courant de drain dépendant de la température avec une énergie d'activation variant linéairement de 0,57 eV à 0,071 eV selon différentes tensions de grille. Deuxièmement, l'impact de l'éclairage sur les TFT PC-ZnO à basse température de 280 K est étudié, manipulant la mobilité électrique et les défauts profonds. Troisièmement, la taille des grains et les effets de limite sur les TFT d'oxyde de zinc nanocristallins sont explorés par le biais d'analyses expérimentales et numériques, démontrant l'influence de la température de dépôt sur la taille des grains et les caractéristiques de transfert ultérieures. Enfin, les TFT constitués de films minces de ZnO déposés sur divers substrats sont étudiés, détaillant le processus de dépôt, le contrôle de la pression et les conditions de recuit. La recherche fournit des informations précieuses sur l'optimisation des performances des TFT à base de ZnO pour les applications électroniques.

Mots clés : Elaboration, Caractérisation, Conception, TFT, SILVACO ATLAS, Défauts.

الملخص

تستكشف الأطروحة مجال أكاسيد أشباه الموصلات متعددة البلورات، وخاصة أكسيد الزنك (ZnO)، كعنصر رئيسي في ترانزستورات الأغشية الرقيقة (TFTs) الضرورية للتطبيقات الإلكترونية مثل شاشات الكريستال السائل النشطة المصفوفة (AMLCDs). باستخدام عمليات المحاكاة العددية مع SILVACO ATLAS، تبحث الدراسة في أربعة مجالات رئيسية. أولاً، تم فحص تأثير درجة الحرارة على PC-ZnO TFTs، مما يكشف عن تيار تصريف يعتمد على درجة الحرارة مع طاقة تنشيط تتراوح خطيًا من 0.57 eV إلى 0.071 الكترون فولت عبر الفولتية المختلفة للبوابة. ثانيًا، تمت دراسة تأثير الإضاءة على PC-ZnO TFTs عند درجة حرارة منخفضة تبلغ 280 كلفن، ومعالجة الحركة الكهربائية والعيوب العميقة. ثالثًا، يتم استكشاف حجم الحبوب وتأثيراتها الحدودية على TFTs لأكسيد الزنك البلوري النانوي من خلال التحليل التجريبي والعددي، مما يدل على تأثير درجة حرارة الترسيب على حجم الحبوب وخصائص النقل اللاحقة. وأخيرًا، تم فحص TFTs المصنوعة من أغشية ZnO الرقيقة المودعة على ركائز مختلفة، مع تقديم تفاصيل عملية الترسيب والتحكم في الضغط وظروف التلدين. يوفر البحث رؤى قيمة لتحسين أداء TFTs المستندة إلى ZnO للتطبيقات الإلكترونية.

الكلمات المفتاحية: أكسيد الزنك، TFT، رواسب الأغشية الرقيقة، سيلفاكو ATLAS ، العيوب.

Table of Contents

List of Figures

List of Tables

General introduction

Thin film transistors (TFTs) play an important role in today's flat-panel displays (FPDs) due to unique characteristics of oxide semiconductors such as zinc oxide (ZnO) [1]. The advantages of FPDs are obvious, especially for portable applications such as laptop computers, medical imaging X-ray sensors, and avionic displays. Today, it is also clear that the heavy and bulky CRTs will soon become history just like their other vacuum counterparts. In fact, the commercial battle between the cathode ray tubes (CRTs) and FPDs is very intense. The main reason for FPDs' not having completely taken over the CRT market is that they cost more than CRTs, but the gap is closing every year [2].

Oxide semiconductors are widely researched for applications in TFTs because of the relatively low-cost compared the mature a-Si TFT technology [3]. Polycrystalline ZnO or GaInZnO (GIZO) channel are being investigated for advanced applications such as all-transparent electronics and displays [4]-[5]. We can be severely degraded by different types of stress such as negative or positive bias, temperature, exposure to light or even mechanical strain [6]-[7]. Although the ZnO TFT performance has been greatly improved, its physical properties are still not well understood. In particular, the lack of modeling and simulation of ZnO TFTs [8]-[9]. The advantage of using numerical simulation is that it can provide information and explain physical phenomena that are difficult to achieve by measurement [10].

In polycrystalline ZnO, like a-Si, the states are continuously distributed in its energy gap to model the measured or modeled characteristics of TFTs [11]. Temperature has a very remarkable effect on these characteristics, yet the work in this area is very limited [12]. In this thesis, a detailed numerical simulation is carried out to elucidate the experimental behavior of the temperature dependent characteristics current-voltage (I-V) characteristics of the polycrystalline zinc oxide thin film transistor (pc-ZnO TFT). The temperature dependence of the TFT parameters (threshold voltage and the field effect mobility) was also clarified.

Like any semiconductor devices, TFTs are very sensitive to stress optical at deep defects and this dependence can lead to the understanding of the conduction phenomena. To the author's knowledge, a limited work is carried to the effect of temperature on ZnO TFTs [12]. Realizing stable ZnO-based TFTs with both decent mobility and I_{on}/I_{off} ratio still requires much more effort in searching for the appropriate fabrication conditions [13]. In this thesis, we study the effect of modality illumination on the current-voltage (I-V) characteristics of a thin film

transistor based on polycrystalline zinc oxide (pc-ZnO TFT).

Low-temperature-deposited ZnO films are monocrystalline in nature with grain size ranging from 50 to 100 nm, consequently, contains a large number of grain boundaries (GBs). It was shown that polycrystalline ZnO TFT, can show a field-effect mobility (μ_{FE}) as high as 7 cm^2/Vs [8]. Nano-crystalline ZnO TFT (by some of the current authors), has achieved higher field-effect mobility of ~25 cm^2/Vs at 250℃ and grain size ranging from 65 to 95 nm deposited by ALD. Numerical simulation is a powerful tool for understanding and optimizing TFT performance, allowing systematic studies of different parameters and designs the device that is experimentally infeasible [10]. The objective of this work is to use a physically based two-dimensional simulator ATLAS (Silvaco 2018) as a tool to investigate the effects of grains and GB trap states on ZnO-TFT at various temperatures and to determine the mechanism of the carrier carrier's transportation across the channel between the grains nano-crystalline ZnO for different lengths grain (Lg) in ZnO TFTs.

We fabricated of Zinc Oxide (ZnO) Thin Film Transistors (TFTs) with Hafnium Dioxide (HfO_2) and Aluminum Oxide (Al_2O_3) gate insulators involved several steps, including the deposition of ZnO thin films on 100 nm-thick HfO_2 and Al_2O_3 gate insulators.

In general, the deposition of a ZnO semiconductor layer in thin-film transistors (TFTs) is typically performed at high temperatures to achieve improved crystalline quality and lower contact resistance[14]. However, this approach limits the use of lightweight, flexible, and plastic substrates. To overcome this limitation, various transparent oxide semiconductor-based transistors have been proposed[15], employing ZnO as the channel layer deposited at lower temperatures. Although these transistors exhibit relatively low channel mobility ranging from 1 to 3 cm^2/Vs, achieving high performance in low-temperature-grown ZnO TFTs is not the sole concern. One of the major challenges associated with ZnO TFTs is the presence of donor defects, which can significantly impact their overall performance.

This thesis contains four chapters. In the first chapter zinc oxide properties and deposit methods are presented. Second chapter deals with history and operation at the thin film transistors. The simulation of ZnO TFT is presented in the third chapter. Finally, the fourth chapter details the results obtained in this thesis and their discussion. This thesis finishes with a conclusion.

Chapter I: Zinc oxide properties and deposit methods

I.1 Introduction

Zinc oxide (ZnO) has sparked interest, in the field of thin film transistor (TFT) research due to its properties such as high electron mobility, see through quality, and suitability for low temperature deposition techniques.

The concept of thin film technology can be traced back to times when practices like gold beating were used to create thin layers of gold. Essentially, thin films consist of materials that're significantly thinner in the micrometer range, giving them a quasi-two-dimensional quality. This reduction, in thickness influences the characteristics of the material, where boundary effects play a significant role compared to bulk materials.

I.2 The Zinc Oxide

Zinc oxide (ZnO) is a wide-bandgap semiconductor material that has gained considerable attention in the development of thin-film transistors (TFTs) due to its high electron mobility, transparency, and compatibility with low-temperature deposition techniques.

ZnO TFTs have several advantages over other TFT technologies, including high mobility, high on/off current ratio, low leakage current, and excellent stability under prolonged operation. Additionally, ZnO TFTs can be fabricated using a variety of deposition techniques, such as sputtering, chemical vapor deposition, and sol-gel, which offer flexibility in device design and fabrication.

The electrical properties of ZnO TFTs are strongly dependent on the deposition method, film thickness, and annealing conditions. The use of high-quality ZnO thin films is crucial for achieving high-performance TFTs, and several methods have been developed for the characterization of ZnO thin films in TFT applications.

I.2.1 Properties of zinc oxide

Zinc oxide (ZnO) is a versatile and important semiconductor material with a wide range of properties that make it attractive for various applications. ZnO has two main crystal structures, the hexagonal wurtzite and cubic zincblende. However, the wurtzite phase is more commonly observed in ZnO thin films and nanomaterials due to its lower energy state.

ZnO is typically an n-type semiconductor with a bandgap energy of around 3.37 eV. In terms of its chemical and structural properties, ZnO is a white powder that is insoluble in water and has a melting point of around 1975°C [16]. It is chemically stable in air, but can react with acids and strong oxidizing agents. ZnO thin films can be deposited using various methods. Optically, ZnO exhibits strong light absorption and luminescence properties, making it useful in photonic applications, such as light-emitting diodes and sensors. Additionally, ZnO thin films exhibit good transparency in the visible region, making them attractive for applications in transparent electrodes. Electrically, ZnO is a wide-bandgap semiconductor with high electron mobility, making it attractive for high-speed electronic devices. The electrical conductivity and field-effect mobility of ZnO can be enhanced by doping and optimizing the microstructure of the thin film.

Finally, the interface properties of ZnO are important for its performance in electronic devices. The interface between ZnO and other materials, such as metals or organic semiconductors, can strongly influence the electronic properties of the device, and therefore, understanding and optimizing these interface properties is critical for achieving high-performance devices.

I.2.1.1 Evolution of ZnO in research

Zinc oxide has been investigated already in 1912. With the beginning of the semiconductor age after the invention of the transistor [17], systematic investigations of ZnO as a compound semiconductor were performed. In 1960, the good piezoelectric properties of zinc oxide were discovered[18], which led to the first electronic application of zinc oxide as a thin layer for surface acoustic wave devices [19].

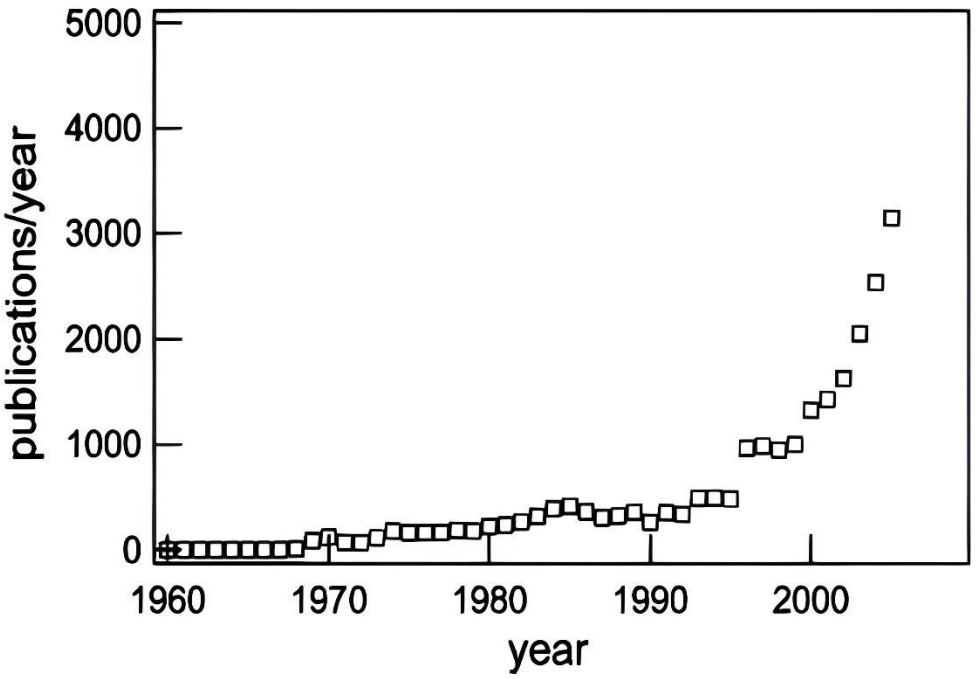


Figure I-1:Increase of the number of publications about zinc oxide (ZnO) over the last 40 years according to the literature data base SCOPUS [20].

I.2.1.2 The zincite

Zinc oxide (ZnO) is classified as a compound semiconductor belonging to the II-VI group. It is naturally present in the form of a mineral called zincite, which exhibits various colors depending on the impurities it contains (as shown in Figure I-2). ZnO has an oxidic composition and occurs as a rare mineral that adopts the hexagonal wurtzite crystal structure with the space group P63mc [21]. The mineral zincite was first discovered by Bruce in 1810 in Franklin, New Jersey. It is primarily found in zinc ore deposits and is often associated with other minerals such as sphalerite and pyrite.

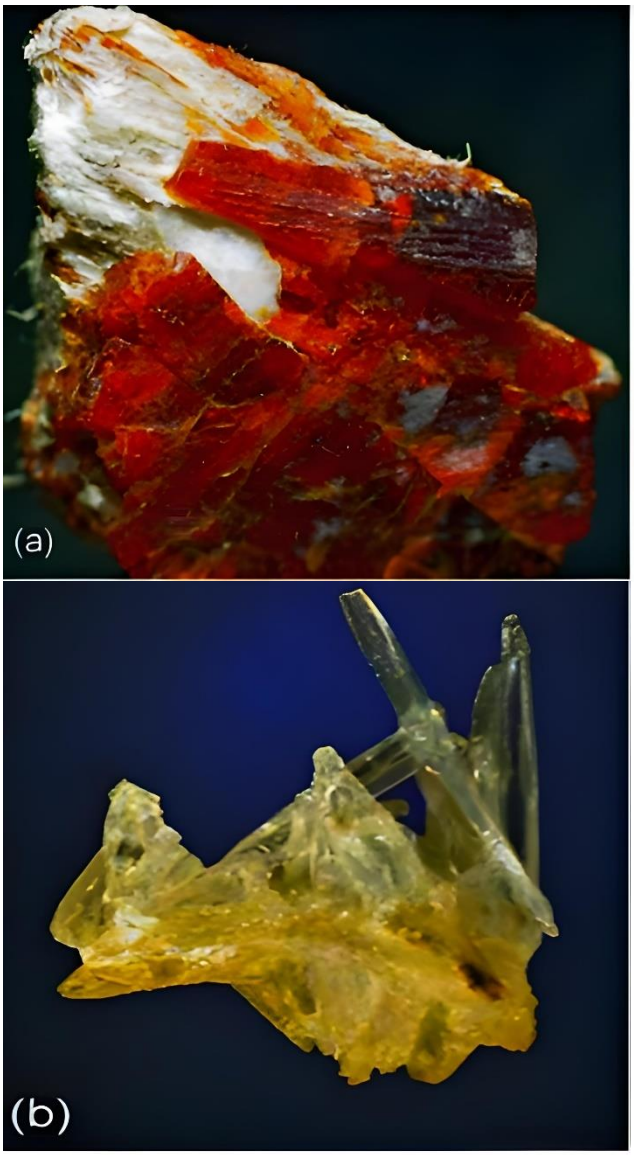


Figure I-2:(**a**) An orange zincite crystal from Sterling Mine, Ogdensburg, USA and (**b**) a synthetic zinc oxide crystal.

New Jersey holds significant importance as a major zinc source in the United States, while other regions such as Sarawezza (Tuscany, Italy), Tsumeb (Namibia), Olkusz (Poland), Spain, Tasmania, and Australia are also known for their zincite deposits. Notably, the Bejaia region in Algeria hosts large-scale mines that have recently been actively exploited. Manganese impurities commonly give zincite its characteristic red or orange coloration. Visual representations of zincite can be observed in Figure I-2. Presently, the majority of globally produced zinc oxide powder is primarily utilized in non-electronic applications such as rubber manufacturing, chemical production, paints, agricultural practices, and ceramic applications.

I.2.2 Specific of properties of ZnO

Zinc oxide (ZnO) exhibits various crystal structures, including wurtzite, zinc blende, and rocksalt, as depicted in Figure I-3. Apart from the wurtzite structure, ZnO can also adopt a zincblende crystal structure, which belongs to the face-centered cubic (FCC) crystal system. In this structure, both the zinc and oxide ions are arranged similarly to the wurtzite structure [22]. However, in the zincblende structure, all the available tetrahedral sites are occupied by zinc ions, while the oxide ions occupy all the available octahedral sites. The zincblende structure features a more compact and symmetrical unit cell, and it is commonly observed in other semiconductor materials such as gallium arsenide.

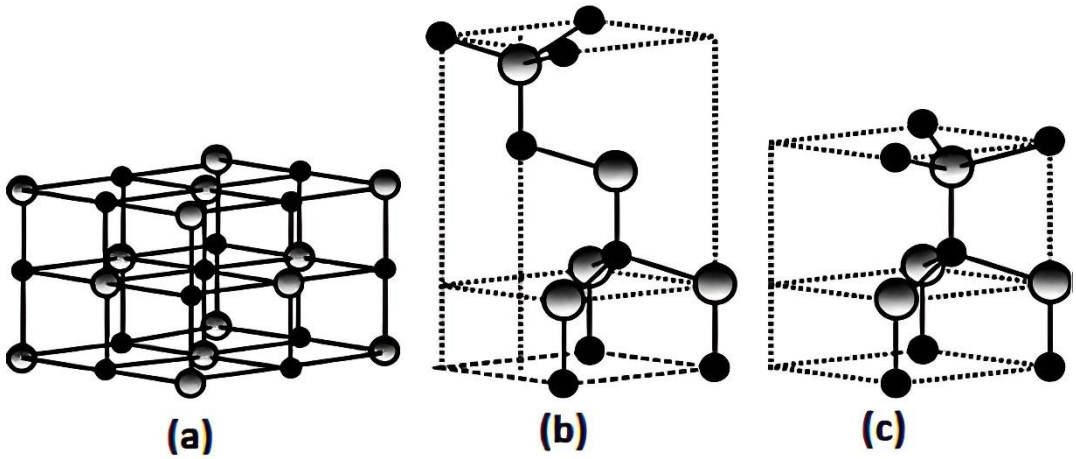


Figure I-3:Stick-and-ball representation of ZnO crystal structures: (a) cubic rocksalt, (b) cubic zinc blende, and (c) hexagonal wurtzite. Shaded gray and black spheres denote Zn and O atoms, respectively.

At ambient conditions, the thermodynamically stable phase is the wurtzite crystal structure, shown schematically in Figure I-4. The wurtzite crystal structure is characterized by a long and narrow unit cell with c-axis as its long axis, and it exhibits a piezoelectric effect.

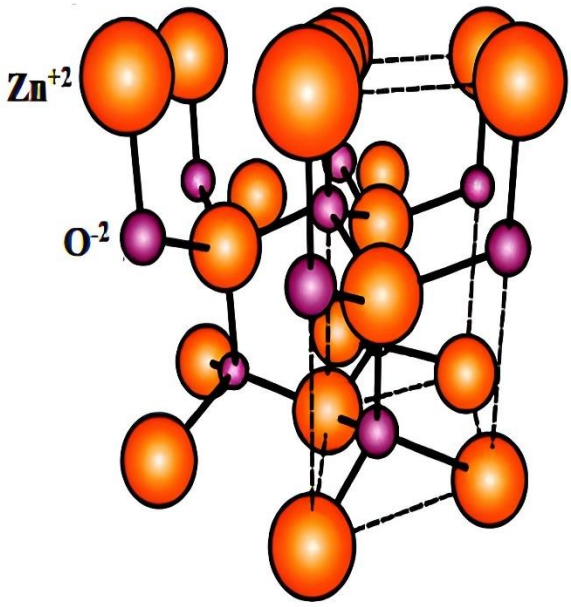


Figure I-4: ZnO in phase the wurtzite crystal structure.

The ZnO bulk crystals have been grown by a number of methods, as has been reviewed recently and large-size ZnO substrates are available [23]. High-quality ZnO films can be grown at relatively low temperatures less than 700 °C [24]-[25]. There has been a great deal of interest in zinc oxide ZnO semiconductor materials lately, as seen from a surge of a relevant number of publications. The interest in ZnO is fueled and fanned by its prospects in optoelectronics applications owing to its direct wide band gap Eg=3.3 eV at 300 K.

Zinc oxide (ZnO) is typically considered an n-type semiconductor due to its tendency to form oxygen-deficient films. While p-type doping of ZnO has been demonstrated experimentally, achieving reliable p-type doping is challenging compared to n-type doping. This difficulty arises from the compensation effects caused by native defects such as zinc interstitials and oxygen vacancies. Poly-crystalline ZnO inherently exhibits n-type conductivity. In addition to its traditional applications, ZnO has found new uses in fields such as transparent thin-film transistors, where the need for a protective covering against light exposure is eliminated due to the material's insensitivity to visible light. ZnO can also accommodate high levels of charge carriers, up to 2.10^{21} cm^{-3}, through heavy substitutional doping. By controlling the doping level, the electrical properties of ZnO can be tailored from insulator to n-type semiconductor or even metal, while maintaining its optical transparency. This characteristic makes ZnO well-suited for applications such as transparent electrodes in flat-panel displays and solar cells. Moreover, ZnO shows promise for utilization in spintronics applications [26].

Chapter I: Zinc oxide properties and deposit methods

Zinc oxide (ZnO) is a highly promising material for blue and ultraviolet optical devices due to its wide bandgap of 3.4 eV and significant exciton binding energy of 60 meV at room temperature. In this application range, ZnO offers several advantages over gallium nitride (GaN), such as a larger exciton binding energy and the ability to grow single crystal substrates. Another notable benefit of ZnO is its broad chemistry, which allows for various wet chemical etching techniques. Additionally, ZnO exhibits a low power threshold for optical pumping, making it energy-efficient. It also possesses radiation hardness and biocompatibility, further enhancing its appeal for device applications. These exceptional properties position ZnO as an ideal candidate for a wide range of devices, including sensors, ultraviolet laser diodes, and nanotechnology-based devices like displays.

Figure I-5 visually depicts the potential energies of the conduction band (CB) and valence band (VB) in ZnO, a direct band gap semiconductor. The top of the VB and the bottom of the CB are highlighted as the energy reference points. When considering the movement of electrons and holes, the kinetic energy of electrons is measured in an upward direction from the CB, while the kinetic energy of holes is measured downward from the VB. This convention is followed because holes possess a charge that is opposite to that of electrons. Both electrons in the CB and holes in the VB play a crucial role in contributing to the flow of current [27].

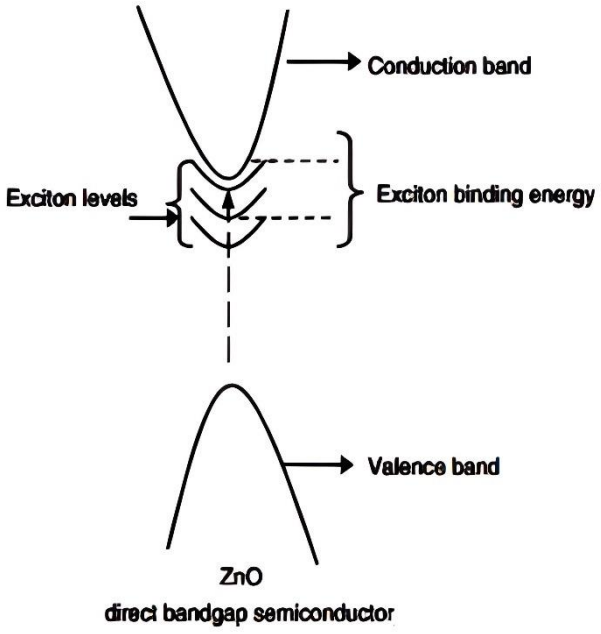


Figure I-5:CB and VB of ZnO.

In the field of solid-state physics, the electronic structure of materials is often described in terms of energy bands, namely the conduction band (CB) and valence band (VB). In the case of ZnO, the valence band consists mainly of electrons occupying the 2p orbitals of oxygen atoms and the 4s orbitals of zinc atoms. These electrons are tightly bound to their respective atoms and form covalent bonds that connect them. On the other hand, the conduction band is primarily formed by delocalized states originating from the 4s and 4p orbitals of the zinc atoms. These electrons have a higher degree of freedom and are capable of moving relatively freely within the crystal, contributing to the material's electrical conductivity.

The position of the CB and VB with respect to the Fermi level (the energy level at which electrons have a 50% probability of occupancy) is important in determining the electrical and optical properties of ZnO. In general, when the CB is close to the Fermi level, ZnO exhibits n-type conductivity, meaning that it has an excess of negatively charged electrons. When the VB is close to the Fermi level, ZnO exhibits p-type conductivity, meaning that it has an excess of positively charged "holes" (missing electrons).

Due to the extensive research on the properties of ZnO, the chemical, structural, optical, electrical and interface properties of zinc oxide are summarized with special emphasis on the use of ZnO as a channel transparent in thin-film transistor. This work has a number of requirements that ZnO can meet.

I.2.3 The main advantages of ZnO in TFT

Zinc oxide (ZnO) is a favorable thin-film transistor (TFT) material due to its unique electrical, optical, and material properties. Advantages of using ZnO in TFTs include:

1. High transparency in the visible and near infrared spectral region, making it ideal for use in transparent and flexible electronic applications such as displays and sensors[28].
2. High electron mobility, ZnO has high electron mobility, which means it can transport electrons more efficiently than other materials used in TFTs, such as amorphous silicon or organic semiconductors. This results in faster switching speeds and better device performance[29].
3. Possibility to prepare highly-doped films with free electron density $n > 10^{19}$ cm^{-3} and low resistivity ($<10^{-3}$ Ω cm)[30].
4. Good contacts to the active semiconductors (absorber layers).

5. Compatibility with flexible substrates, ZnO can be deposited on flexile substrates such as plastic and paper, making it suitable for use in flexible electronics applications[31].
6. Chemical stability, ZnO is chemically steady and resistant to degradation, making it suitable for harsh environments and utilization requiring long-term stability[32].
7. Possibility to prepare the channels on short areas by deposition methods like magnetron sputtering or metal-organic chemical vapor deposition (MOCVD)[33].
8. Possibility to prepare ZnO films with suitable properties at low substrate temperature (<200◦C for insulator oxides TFT)[34].
9. Low material costs, nontoxicity, and abundance in earth crust.
10. Considering that ZnO has many unique properties, it has been used in a variety of applications such as light-emitting diodes[35], lasers [36], piezoelectric transducers, variators [23], photolysis of environmental pollutants[37], and solar cells[38], and chemical sensors[39]. Recently, they have been significantly used in TFT.

I.3 Thin film of Zinc Oxide

A thin film of ZnO is a layer of ZnO material that has a thickness on the order of nanometers to micrometers. These thin films can be produced using various deposition techniques, such as sputtering, chemical vapor deposition, and sol-gel processing.

ZnO thin films have received significant attention in recent years due to their unique properties and potential applications. For example, ZnO thin films can exhibit high transparency in the visible region of the electromagnetic spectrum, while also being able to absorb and emit ultraviolet light, making them useful for applications in transparent electronics, such as touchscreens and solar cells. The properties and potential applications of ZnO thin films make them a promising material for various fields, including electronics, photonics, and optoelectronics. The ability to control the properties and morphology of ZnO thin films through various deposition techniques and processing methods provides a great deal of flexibility in tailoring the properties of the material for specific applications [40].

I.3.1 Thin-film technology

Thin-film technology is simultaneously one of the oldest arts and one of the newest sciences. Involvement with thin film dates to the metal ages of antiquity. Consider the ancient craft of gold beating, which has been practiced continuously for at least four millennia. Gold's great malleability enables it to be hammered into leaf of extraordinary thinness while its beauty and resistance to chemical degradation have earmarked its use for durable ornamentation and

protection purposes [25].

In essence, a thin layer of a particular material is a component of that material with one dimension, known as thickness, significantly reduced, while keeping the other dimensions unchanged. The thickness is typically in the range of micrometers (µm), giving the layer a quasi-two-dimensional nature. This reduction in dimensionality leads to significant alterations in the material's physical properties. The fundamental distinction between the bulk material and thin layers lies in the role played by the boundaries. In the bulk state, the properties are influenced by the bulk material itself, whereas in thin layers, the effects related to the boundary surfaces become predominant. It is evident that as the thickness decreases, the two-dimensional effects become more prominent. However, once the thickness exceeds a certain threshold, these effects become minimal, and the material regains its well-known properties observed in bulk form.

I.3.2 Concept thin film

A "thin film" refers to a solid or liquid object in which one of its dimensions is significantly smaller than the other two. When the growth of the film occurs atom by atom or molecule by molecule, it is classified as a thin film. Conversely, if the growth takes place grain by grain, it is referred to as a thick film. It is challenging to establish a precise boundary between thin and thick films, although some literature arbitrarily defines it as 1 µm. In essence, a film is considered "thin" when its properties exhibit significant deviations from those of the bulk material [41].

Thin films can be made from a wide range of materials, including metals, semiconductors, oxides, polymers, and organic compounds. By controlling the deposition process and parameters, engineers and scientists can tailor the properties of thin films to meet specific requirements. For example, thin films can be engineered to be transparent, conductive, reflective, or protective, depending on the intended application.

Some examples of thin film applications include semiconductor devices like thin-film transistors (TFTs) used in flat-panel displays, solar cells, optical coatings on lenses and mirrors, protective coatings on cutting tools or electronic components, and magnetic thin films used in data storage devices like hard drives.

I.3.3 The importance of thin films in various fields

The significance of thin films stems from their ability to exhibit distinct properties that differ from their bulk counterparts. The nanoscale thickness of thin films allows for precise control and manipulation of their optical, electrical, magnetic, and mechanical properties. This control is crucial for tailoring materials to meet specific requirements in diverse applications.

In electronics, thin films are used to create components such as transistors, interconnects, and displays. They enable the miniaturization of devices and the integration of multiple functionalities into compact systems. Thin film technologies have revolutionized the electronics industry, contributing to the development of smartphones, computers, and other portable devices.

Optics and photonics heavily rely on thin films to manipulate light and enhance optical properties. Thin film coatings are utilized in anti-reflective coatings, mirrors, filters, and optical waveguides[42]. They enable precise control of light transmission, reflection, and absorption, facilitating advancements in telecommunications, solar cells, imaging systems, and laser technologies.

Thin films find extensive use in the field of energy as well [43]. They are employed in solar cells to absorb and convert sunlight into electricity. Thin film batteries and supercapacitors provide energy storage solutions for portable electronics and electric vehicles. Thin film coatings are also used in energy-efficient windows and building materials to regulate heat transfer.

Other fields benefiting from thin films include catalysis [44], where thin films provide enhanced surface area and reactivity for efficient chemical reactions. Thin films are utilized in sensors, enabling precise detection of gases, humidity, temperature, and biological analytes. Additionally, thin film coatings offer protective and corrosion-resistant layers in aerospace, automotive, and manufacturing industries.

In summary, thin films offer unique properties and capabilities due to their nanoscale thickness, making them indispensable in various fields. They enable advancements in electronics, optics, energy, sensing, and more. The ability to precisely engineer thin film properties has opened up new possibilities for technological innovations and continues to drive

research and development in numerous industries.

I.3.4 Zinc Oxide is a material suitable for thin film applications

Zinc Oxide (ZnO) is a highly suitable material for thin film applications due to its unique properties and versatile characteristics. Firstly, ZnO possesses a wide bandgap energy, making it transparent to visible light while exhibiting strong absorption in the ultraviolet (UV) region. This property is advantageous for applications such as transparent conductive films, ultraviolet sensors, and photodetectors. Additionally, ZnO demonstrates high electron mobility, enabling the fabrication of high-performance thin film transistors (TFTs) used in electronic displays and integrated circuits. Its piezoelectric properties make it suitable for applications in sensors, actuators, energy harvesting devices, and piezoelectric resonators.

ZnO exhibits excellent chemical and thermal stability, making it compatible with diverse deposition techniques and substrate materials. It can withstand high temperatures during thin film fabrication processes, ensuring stability and durability in demanding operating conditions [45]. The material's biocompatibility makes it non-toxic and suitable for biomedical applications such as antibacterial coatings, drug delivery systems, and biosensors. ZnO thin films also possess interesting optical properties, including high transparency in the visible spectrum and strong UV absorption. These properties enable their use in anti-reflective coatings, optical waveguides, and light-emitting devices. Furthermore, ZnO thin films can be deposited using various techniques such as physical vapor deposition (PVD), chemical vapor deposition (CVD), pulsed laser deposition (PLD), and sol-gel methods. This versatility allows for the fabrication of ZnO thin films on different substrates with controllable thickness and properties.

General, ZnO has a wide bandgap, high electron mobility, piezoelectricity, stability, biocompatibility, optical properties, and deposition versatility make it a highly suitable material for thin film applications in electronics, optics, energy, sensing, biomedicine, and more. Its unique properties continue to drive research and development, opening up new possibilities for technological advancements in various fields[46].

I.3.5 Deposition techniques ZnO thin film

Deposition techniques for ZnO thin films can be broadly categorized into two main

categories: physical methods (PVD) and chemical methods (CVD). Physical methods involve the physical transfer of material from a source to a substrate, while chemical methods rely on chemical reactions to deposit the thin film. Each category encompasses several specific techniques, each with its advantages and limitations.

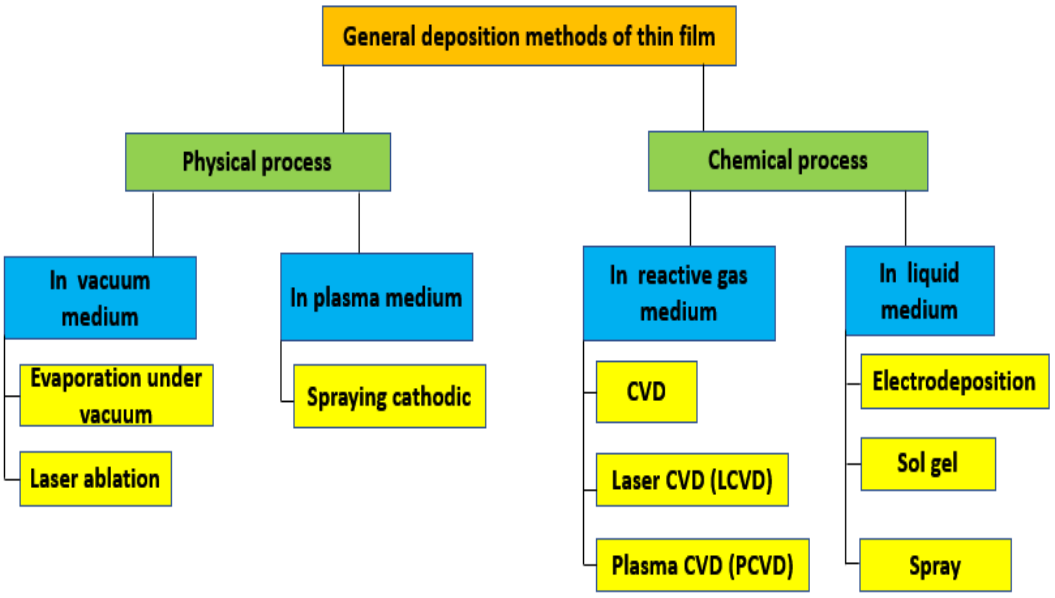


Figure I-6:different methods of deposit.

Physical Vapor Deposition (PVD) techniques for ZnO thin film deposition include evaporation under vacuum, cathodic spraying, and laser ablation. These techniques involve the vaporization of a solid ZnO source material or the bombardment of a ZnO target to generate a vapor that condenses onto the substrate, forming a thin film. PVD methods offer control over film thickness, composition, and uniformity, making them suitable for precise deposition.

Chemical vapor deposition (CVD) techniques for deposition of ZnO thin films include methods such as metallurgical chemical vapor deposition (MOCVD), atomic layer deposition (ALD), and plasma-enhanced chemical vapor deposition (PECVD). These techniques involve introducing gaseous precursors onto a heated substrate, where chemical reactions occur to precipitate the ZnO thin film. And also, we have liquid medium technologies, sol gel and spray. CVD methods provide precise control over film properties, uniformity, and the ability to deposit films on complex structures.

The selection of deposition techniques for ZnO thin films depends on various factors, including the desired film properties, deposition control, scalability, substrate compatibility,

and application requirements. Researchers and engineers must carefully consider these factors to determine the most suitable deposition technique for their specific needs.

In this context, understanding and exploring the available deposition techniques for ZnO thin films are crucial for achieving desired film quality, uniformity, and functionality. The appropriate choice of deposition method can enable the realization of ZnO thin films with tailored properties to meet the demands of diverse applications in electronics, optics, sensors, and beyond.

I.3.6 Some deposit techniques

Zinc oxide (ZnO) is a promising material for thin-film transistors (TFTs) due to its high electron mobility, transparency, and low cost. There are several deposition techniques available for depositing ZnO thin films, each with its own advantages and disadvantages. In this thesis, we will discuss some of the commonly used deposition techniques for ZnO TFTs, including DC deposition, laser ablation, sputtering, and sol-gel.

I.3.6.1 DC deposition

DC deposition is a physical vapor deposition technique used to deposit thin films of materials onto a substrate. In this process, a target material is placed in a vacuum chamber, and an electric current is applied to it, causing it to vaporize and form a plasma. The plasma then condenses onto the substrate, forming a thin film.

The vacuum chamber used in DC deposition is typically a high-vacuum system, with pressures in the range of 10^{-4} to 10^{-6} Torr. This low-pressure environment is necessary to prevent the deposition of impurities and to ensure the purity of the deposited film [47]. The target material used in DC deposition can be any material that can be vaporized by the application of an electric current. Common target materials include metals, semiconductors, and insulators. The target material is typically a solid or powder that is placed in a crucible or on a target holder in the vacuum chamber.

To initiate the deposition process, a high voltage is applied to the target material, creating an electric field that ionizes the gas molecules in the chamber. The resulting plasma consists of positively charged ions, negatively charged electrons, and neutral gas molecules.

The positively charged ions are attracted to the negatively charged substrate, where they condense and form a thin film. The thickness and composition of the deposited film can be controlled by adjusting the deposition time, the power of the electric current, and the distance between the target material and the substrate. In addition, the use of different target materials or gas mixtures can be used to deposit films with different properties.

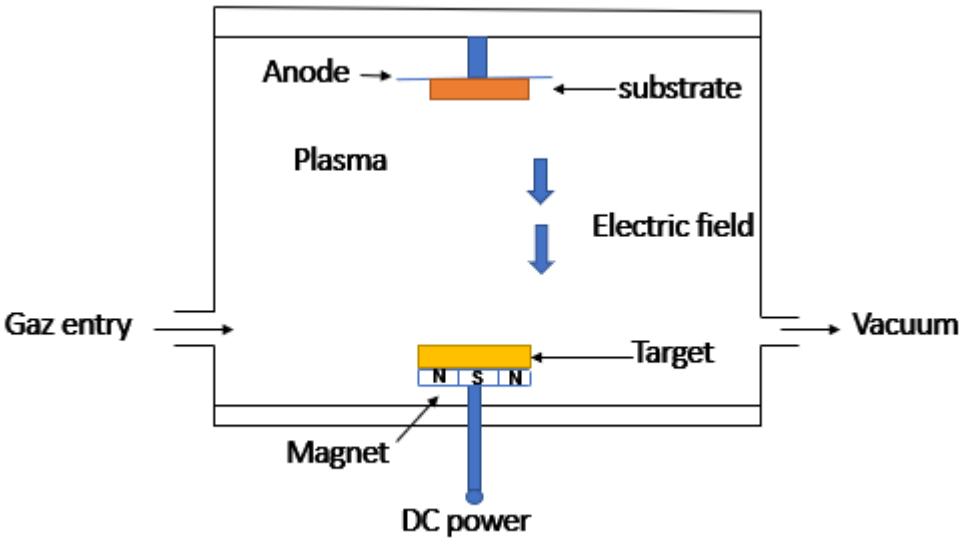


Figure I-7:Schematic of DC deposition.

DC deposition is commonly used in the fabrication of electronic devices such as thin film transistors (TFTs) and solar cells. In the fabrication of TFTs, DC deposition is used to deposit the source, drain, and gate electrodes, as well as the semiconductor and insulator layers. In the case of solar cells, DC deposition is used to deposit the semiconductor layer, which is typically made of silicon, cadmium telluride, or other materials[48].

I.3.6.2 Laser ablation

Pulsed Laser Deposition (PLD) is a depot technique that uses a pulsed laser beam. The beam is focused on a target placed in an ultrahigh vacuum chamber. The laser pulses allow the vaporization of materials in the form of plasma. The plume of material thus ejected perpendicular to the target is condensed on a substrate placed opposite to form a coating. This contains a wide variety of chemical species.

This technique has been known for a long time, has proven its effectiveness in depositing a wide variety of materials. The benefits of PLD are multiple. It is a laboratory

process that allows the deposition of a multitude of high purity compounds ranging from high temperature superconductors to hard materials. The purity of the deposits depends, in this case, only on the purity of the target used.

The main advantage of this technique is the deposition at room temperature thus allowing coating on all types of substrates ranging from semiconductors to polymeric materials. One of the very promising applications of the laser ablation process is the production of wear-resistant DLC films. The lasers used generally deliver short pulses of nanosecond (ns) or ultra-short duration of the order of a few hundred femtoseconds [49].

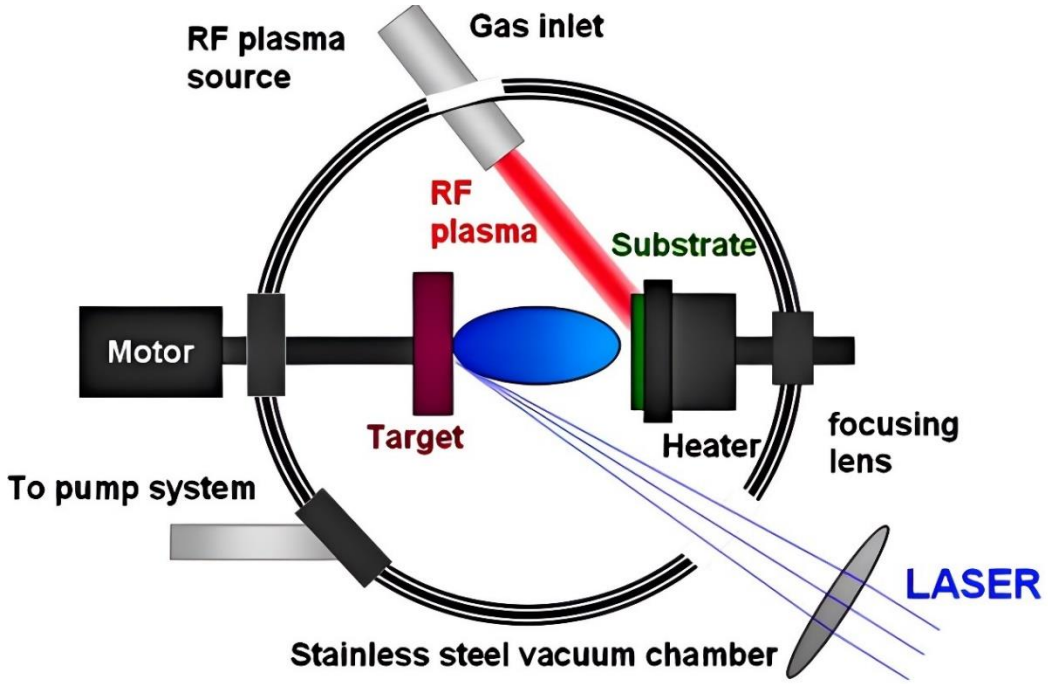


Figure I-8:Diagram of Laser ablation [50].

One advantage of laser ablation is its ability to deposit high-quality thin films with good control over the film properties, such as the thickness, composition, and crystallinity. Additionally, ablation can be used to deposit films on a variety of substrates, including flexible and non-conventional substrates.

I.3.6.3 Sputtering

In this method, the substrate is placed in a chamber containing a gas (usually Argon) at low pressure, in which an electric discharge is caused. This discharge has the role of ionizing the gas atoms. The ions thus obtained are accelerated by a potential difference and come to

bombard a cathode made of the material to be deposited (target). Under the impact of accelerated ions, atoms are torn off the cathode and deposited on the substrate. In some cases, a gas is introduced into the chamber in addition to argon, which will react chemically with the atomized atoms to form the material that it is desired to obtain. Then, we have a reactive cathode sputtering. This method makes it possible to have low resistivity deposits and layers of good stoichiometry having an average transmission in the visible [51].

The advantage of the sputtering method is that it can produce deposits under controlled atmospheres. However, the high cost of the installation, associated with a low production rate makes the sputtering a technique reserved for specific applications reduced.

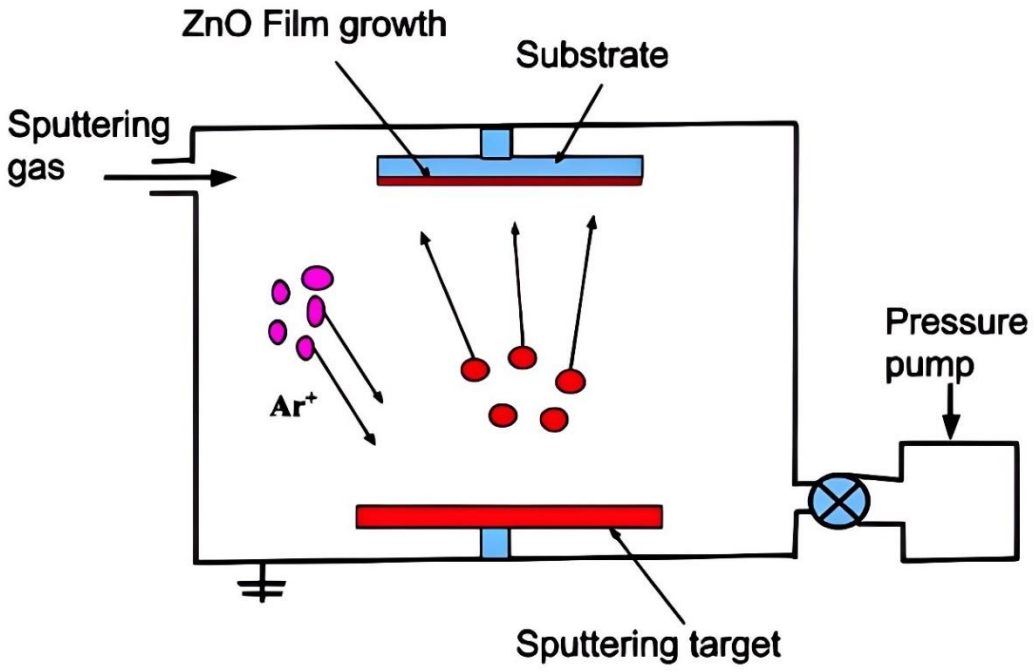


Figure I-9:Schematic of the sputtering.

The advantage of sputtering is its ability to deposit high-quality ZnO thin films with good control over the film properties, such as the thickness and composition. Additionally, sputtering can be used to deposit films on a variety of substrates, including flexible and non-conventional substrates.

I.3.6.4 Sol-gel

Deposition of Zinc Oxide (ZnO) thin films using sol-gel techniques offers a versatile and cost-effective method for fabricating thin films with controlled properties. Among the sol-

gel techniques, two commonly employed methods for depositing ZnO thin films are spin-coating and dip-coating.

The sol-gel process is one of the chemical ways of preparing metal oxide materials such as ceramics and glasses. It consists first of all in the development of a stable suspension (SOL) from chemical precursors in solution. These "soils" will evolve during the gelling step as a result of interactions between the suspended species and the solvent, to give rise to a three-dimensional solid network expanded through the liquid medium. The system is then in the "GEL" state. These so-called "wet" gels are then converted into amorphous dry matter by evacuation of the solvents (an airgel is then obtained) or by simple evaporation under atmospheric pressure (xerogel). The deposit itself can be done in two different ways:

Spin-coating is a widely used sol-gel technique that involves spinning a substrate at high speeds while applying a liquid coating solution. During the spin-coating process, the ZnO precursor solution is dispensed onto the spinning substrate, typically centered on a spin chuck. As the substrate spins rapidly, centrifugal forces spread the solution uniformly across the substrate surface, forming a thin and homogeneous wet layer. Subsequent heating or annealing converts the wet layer into a solid ZnO thin film. Spin-coating provides excellent control over film thickness, uniformity, and morphology, making it suitable for various applications in electronics, optoelectronics, and sensors.

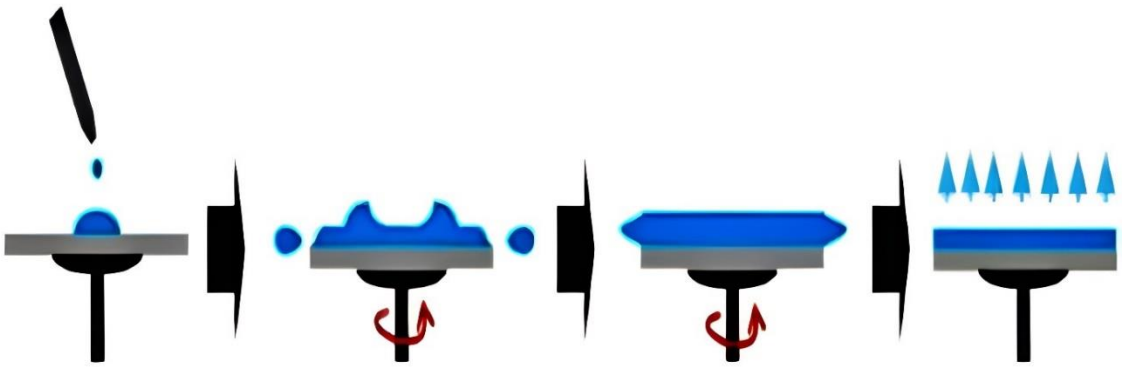


Figure I-10:The four steps of spin coating.

Spin-coating or centrifugation Figure I-10 is to pour the soil or the gel on a substrate rotated by a spin. The excess liquid is ejected under the action of the centrifugal force, and the thickness of the deposit is then a function of the rotational speed of the substrate and the

deposition time.

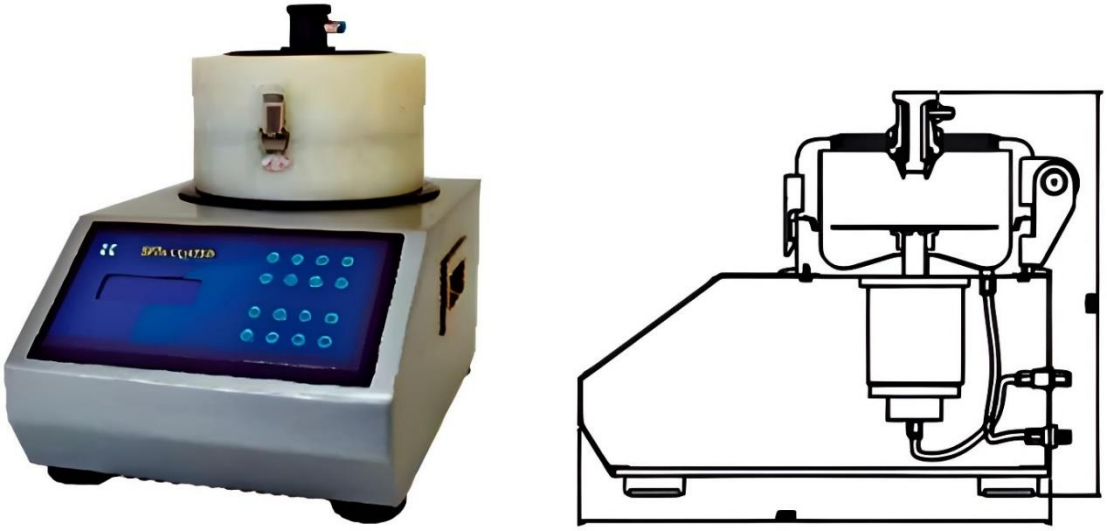


Figure I-11:Holmarc spin coater.

Holmarc Spin Coater is a specialized equipment designed for spin coating applications in the field of thin film deposition. Spin coating is a widely used technique for creating uniform thin films on substrates by rapidly spinning them while dispensing a liquid coating material. The Holmarc spin coater features a robust and compact design that provides precise control over spin speed, acceleration, and coating time. It typically consists of the following components:

1. Spin chuck: The spin chuck holds the substrate securely in place during the spin coating process. It ensures that the substrate remains centered and evenly coated.
2. Motorized spindle: The motorized spindle is responsible for rotating the spin chuck and the substrate at high speeds. The spin speed can be controlled within a wide range to achieve the desired film thickness and uniformity.
3. Coating dispensing system: The spin coater includes a dispensing system to accurately dispense the liquid coating material onto the spinning substrate. This can be achieved through a variety of methods, such as a syringe pump or a pipette.
4. Programmable controller: The spin coater is equipped with a programmable controller that allows users to set and control various parameters such as spin speed, acceleration, and coating time. This enables precise and repeatable coating processes.
5. Vacuum chuck (optional): Some spin coaters may have an optional vacuum chuck that provides enhanced substrate adhesion during the spin coating process. The vacuum

chuck helps prevent substrate slippage and ensures uniform coating.

The Holmarc spin coater is widely used in research laboratories, academic institutions, and industrial settings for a variety of applications, including the deposition of thin films for electronics, optics, and surface modification. It offers a reliable and efficient solution for achieving uniform and controlled thin film coatings on a range of substrate materials.

Dip-coating, another sol-gel technique, involves immersing a substrate into a ZnO coating solution and subsequently withdrawing it at a controlled speed. As the substrate is lifted from the solution, a wet layer of the ZnO precursor forms on its surface. The thickness of the wet layer can be controlled by adjusting parameters such as withdrawal speed and solution viscosity. Following the withdrawal, solvent evaporation causes the wet layer to gel and form a solid ZnO thin film on the substrate. Dip-coating offers simplicity, cost-effectiveness, and the ability to coat complex-shaped substrates. However, achieving precise control over film thickness and uniformity may be challenging compared to spin-coating. [52].

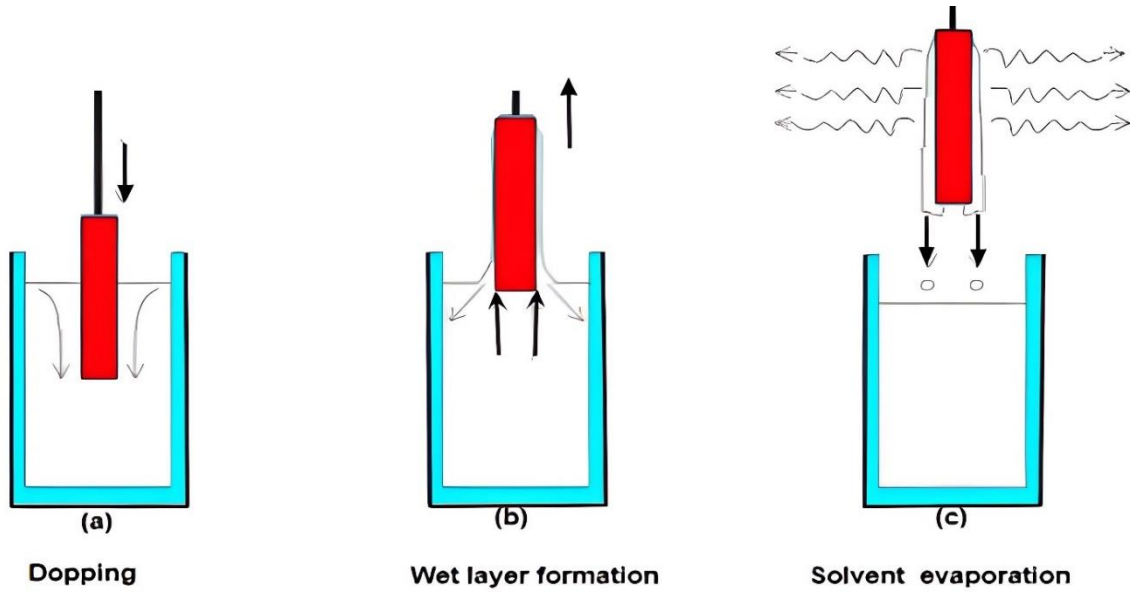


Figure I-12:Stages of the dip-coating process: a) dipping of the substrate into the coating solution; b) wet layer formation by withdrawing the substrate; c) gelation of the layer by solvent evaporation [53].

The dip-coating process involves several stages that contribute to the deposition of a thin film on a substrate. These stages can be summarized as follows:

a) Dipping of the substrate into the coating solution: The first stage of the dip-coating process involves immersing the substrate into a coating solution or liquid film-forming material. The substrate is carefully positioned and dipped into the solution at a controlled speed and angle to ensure uniform coating. The coating solution typically contains the desired material, such as a ZnO precursor, dissolved or dispersed in a suitable solvent.

b) Wet layer formation by withdrawing the substrate: After the substrate is immersed in the coating solution, it is slowly withdrawn at a controlled speed. As the substrate is lifted from the solution, a wet layer or film starts to form on its surface. The thickness of the wet layer depends on factors such as the withdrawal speed, solution viscosity, and substrate properties. The speed and uniformity of the withdrawal process play a crucial role in controlling the thickness and quality of the resulting thin film.

c) Gelation of the layer by solvent evaporation: Once the substrate is withdrawn from the coating solution, the wet layer undergoes a gelation process. This stage involves the evaporation of the solvent present in the coating solution. As the solvent evaporates, the concentration of the film-forming material increases, leading to the formation of a solid or gel-like film. The gelation process enables the formation of a cohesive and adherent thin film on the substrate surface. The duration of the gelation stage can vary depending on the nature of the coating material, solvent properties, and environmental conditions such as temperature and humidity.

It is worth noting that the dip-coating process may involve additional steps, such as rinsing or drying, depending on the specific requirements of the desired thin film. These additional steps can help remove excess coating solution or further enhance the film properties. The dip-coating process involves the sequential stages of substrate immersion, withdrawal to form a wet layer, and subsequent gelation through solvent evaporation. This versatile technique allows for the deposition of uniform thin films with control over film thickness and composition, making it applicable in various fields such as optics, electronics, and surface coatings[54].

I.3.7 Thin layer characterization methods of ZnO

Zinc oxide (ZnO) is a promising material for various applications such as solar cells, gas sensors, and thin-film transistors (TFTs) due to its unique properties such as high electron

mobility, transparency, and low cost. However, the performance of these applications strongly depends on the microstructure and properties of the ZnO thin films. Therefore, thin layer characterization methods are essential to determine the quality and properties of the ZnO thin films. In this thesis, we will discuss some of the commonly used thin layer characterization techniques for ZnO, including Scanning electron microscopy, X-ray diffraction, Diffractometer, and UV-Visible spectroscopy.

I.3.7.1 Scanning electron microscopy (SEM)

Scanning Electron Microscopy (SEM) is a powerful imaging technique commonly employed to analyze the surface morphology, structure, and composition of ZnO thin films. By utilizing a focused electron beam and detecting the emitted secondary electrons, SEM provides high-resolution, three-dimensional imaging of the film's surface topography.

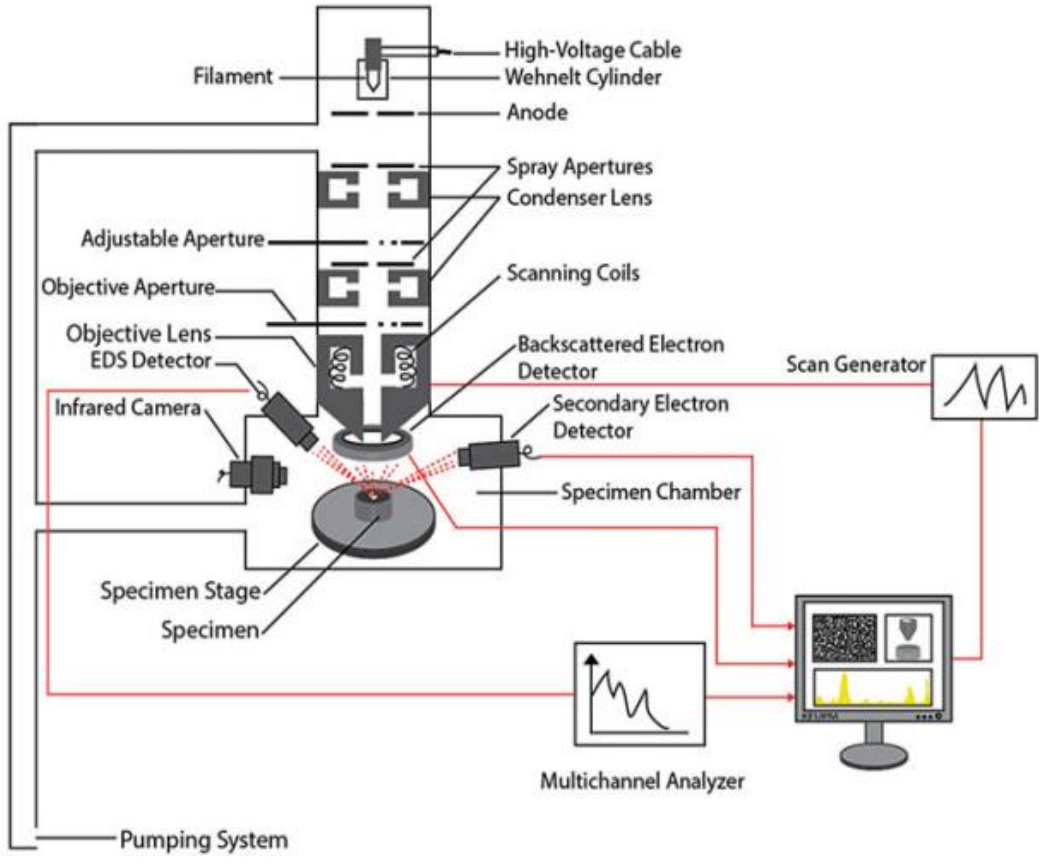


Figure I-13:Diagram showing the different components in SEM [55].

When studying ZnO thin films using SEM, the following steps are typically followed:

1. Sample preparation: The ZnO thin film samples are carefully prepared for SEM

analysis. This involves mounting the thin film onto a suitable substrate and ensuring it is clean and free from contaminants. If necessary, the sample may undergo additional preparation steps such as sputter coating with a thin layer of conductive material (e.g., gold or platinum) to improve image quality and minimize charging effects during SEM imaging.

2. Instrument setup: The SEM instrument is prepared and optimized for imaging ZnO thin films. This includes adjusting the electron beam parameters such as accelerating voltage, beam current, and spot size to obtain the desired resolution and contrast. The instrument is also calibrated using reference samples to ensure accurate measurements.

3. Sample loading: The prepared ZnO thin film sample is carefully mounted onto the SEM stage and positioned for imaging. The stage allows precise control over sample positioning, tilt, and rotation to achieve optimal imaging conditions.

4. Imaging: The electron beam is focused onto the surface of the ZnO thin film, and the emitted secondary electrons are collected to generate an image. SEM provides high-resolution imaging, allowing for detailed examination of the surface morphology, grain boundaries, defects, and features of the ZnO thin film. The imaging parameters, such as beam energy, dwell time, and scan speed, are adjusted to optimize image quality while minimizing beam damage to the sample.

5. Analysis: The acquired SEM images of the ZnO thin film can be further analyzed using various techniques. Image analysis software can be employed to measure film thickness, grain size, and surface roughness. Elemental analysis can also be performed using Energy-Dispersive X-ray Spectroscopy (EDS) coupled with SEM to determine the composition and elemental distribution within the thin film.

SEM analysis of ZnO thin films provides valuable insights into their surface features, morphology, and composition, enabling researchers to assess film quality, understand growth mechanisms, and optimize deposition processes. The information obtained from SEM imaging plays a crucial role in characterizing and tailoring ZnO thin films for specific applications in electronics, optoelectronics, and other fields.

I.3.7.2 Atomic force microscopy (AFM)

Atomic Force Microscopy (AFM) is a powerful imaging technique used to study the surface topography and physical properties of materials at the nanoscale. When applied to ZnO thin films, AFM provides valuable information about their surface morphology, roughness, and other surface-related characteristics. In AFM, a sharp probe with a nanoscale tip is scanned across the sample surface. The interaction between the probe and the surface generates forces that are measured and used to create a three-dimensional image of the surface topography. AFM can operate in various modes, including contact mode, tapping mode, and non-contact mode, depending on the specific requirements of the sample. When applied to ZnO thin films, AFM can reveal important details about the surface features. It can provide information about the grain structure, grain boundaries, and surface defects present in the film. The AFM images can show the individual grains, their size, shape, and arrangement, allowing researchers to assess the quality and uniformity of the thin film.

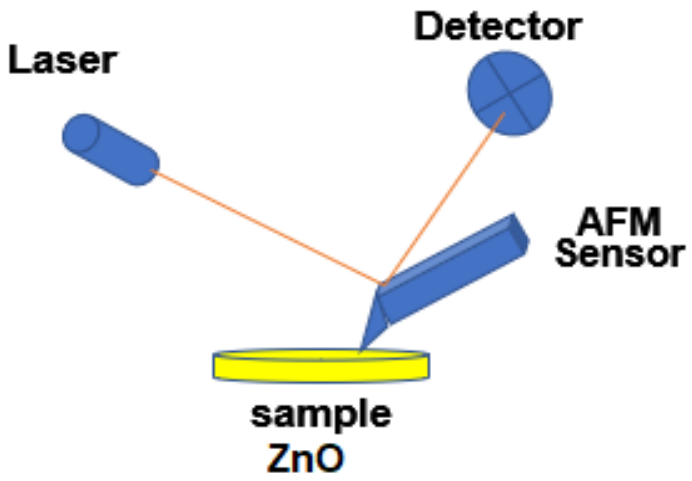


Figure I-14schema of atomic force microscopy (AFM)

When studying ZnO thin films using AFM, the following steps are typically followed:

1. Sample preparation: Prepare the ZnO thin film sample on an appropriate substrate. This may involve techniques such as physical vapor deposition (PVD), chemical vapor deposition (CVD), or sol-gel methods. Ensure that the sample is clean and free from any contaminants.
2. Instrument setup: Set up the AFM instrument in a controlled environment, preferably in a vibration-free room or on an isolation table. Ensure that the instrument is properly

calibrated for accurate measurements.

3. Probe selection: Choose an appropriate AFM probe (also known as a cantilever) for the desired measurement. The choice of probe depends on factors such as the type of measurement (topography, conductivity, etc.), the surface roughness, and the desired spatial resolution.
4. Sample mounting: Mount the ZnO thin film sample onto the AFM stage or sample holder, ensuring secure and stable positioning. The sample should be properly fixed to prevent any movement during scanning.
5. Approach and engage: Use the AFM instrument's control software to approach the sample surface with the probe. The software usually provides feedback on the tip-sample interaction forces, allowing for precise engagement of the probe with the sample surface.
6. Scan parameters: Set the appropriate scanning parameters such as scan size, scan rate, and data acquisition settings. These parameters depend on the specific requirements of the study, such as the desired spatial resolution, imaging speed, and noise levels.
7. Imaging modes: Choose the appropriate imaging mode based on the desired information. AFM offers various modes, including contact mode, tapping mode, and non-contact mode. The selection depends on factors such as sample properties, surface sensitivity, and the type of measurement (topography, conductivity, etc.).
8. Data acquisition: Initiate the scanning process and acquire the AFM data. The instrument records the deflection of the cantilever as it scans the sample surface, capturing the height information and other relevant data.
9. Image analysis: Analyze the acquired AFM data using dedicated software. Process the data to generate three-dimensional topographic images, extract surface roughness parameters, and analyze any other specific features of interest.
10. Interpretation and reporting: Interpret the AFM results, considering the specific objectives of the study. Report and document the findings, including surface morphology, roughness measurements, and any observed surface defects or features. SEM analysis of ZnO thin films provides valuable insights into their surface features, morphology, and composition, enabling researchers to assess film quality, understand growth mechanisms, and optimize deposition processes. The information obtained from SEM imaging plays a crucial role in characterizing and tailoring ZnO thin films for

specific applications in electronics, optoelectronics, and other fields.

I.3.7.3 X-ray diffraction (XRD)

The purpose of this characterization is to study the crystalline structure of the layers, to measure the mesh parameters and the grain size and oxygen vacancy. It must also make it possible to examine the state of the constraints of the deposits.

I.3.7.4 definition

X-ray diffraction techniques are the tools of choice for the analysis of crystallographic problems. They took off from 1912 on which M. von LAUE and his collaborators managed to obtain the first X-ray diffraction diagram by a crystal. The technique evolved very rapidly, but it was not until recent advances in computer science that the powder diffraction technique (giving much more complex diagrams) could be applied in the usual way to the resolution of complex crystalline structures.

I.3.7.5 Principle of X-ray diffraction measurement

X-ray diffraction is a powerful technique for the structural characterization of thin films, including ZnO thin films. In this technique, X-rays are directed onto the sample, and the scattered X-rays are detected and analyzed to determine the structural properties of the sample.

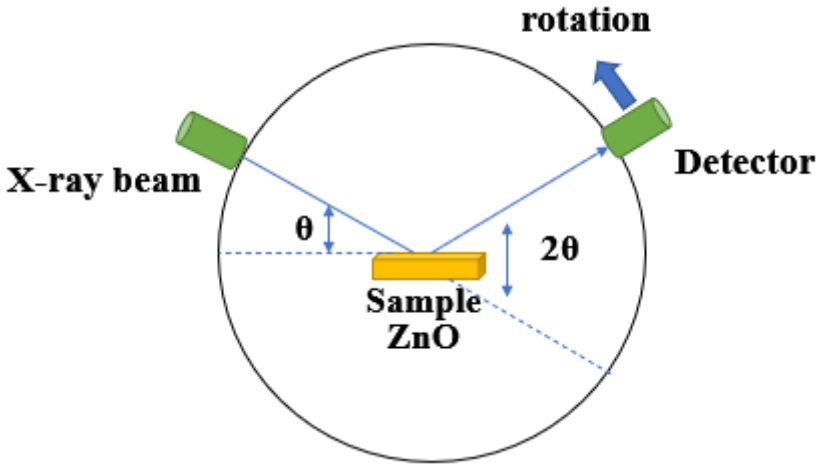


Figure I-15:Experimental X-ray diffraction device.

XRD is commonly used to determine the crystal structure and crystallinity of the ZnO thin films. The diffraction pattern obtained from the ZnO thin films can provide information on the lattice parameters, orientation, and degree of crystallinity. The most commonly observed

diffraction peaks of ZnO correspond to the (002), (100), and (101) planes.

When performing XRD analysis of ZnO thin films, the following steps are typically followed:

1. Sample preparation: The ZnO thin film samples are prepared on a suitable substrate, ensuring cleanliness and freedom from contaminants. The thin film may be deposited using various techniques such as sputtering, chemical vapor deposition, or sol-gel methods. The sample is prepared for XRD analysis by mounting it onto a sample holder or stage.

2. Instrument setup: The XRD instrument is prepared and calibrated for the analysis of the ZnO thin film. This involves setting up the X-ray source, detector, and sample stage. The XRD parameters, such as the type of X-ray radiation, scan speed, and scan range, are optimized for the specific sample and desired analysis resolution.

3. Sample alignment: The prepared ZnO thin film sample is carefully aligned on the sample holder or stage, ensuring proper orientation and stability. The stage allows precise control over the sample positioning and movement during the scanning process.

4. XRD measurement: The X-ray source is directed onto the ZnO thin film sample, and the detector measures the diffracted X-ray intensity as a function of the diffraction angle. The XRD scan typically covers a range of diffraction angles, allowing for the determination of the crystallographic orientation, phase purity, and lattice parameters of the thin film.

5. Analysis: The obtained XRD patterns are analyzed using specialized software. The software allows the identification of crystallographic phases and peak fitting to determine the film's crystal structure and grain size. The lattice parameters of the thin film can also be calculated, providing information about the film's strain state and potential applications.

The beam is focused by a receiving slot placed in front of the detector which records the

intensity. The anode of the X-ray beam, the crystallites of the sample participating in the diffraction and the slit of the detector are on the focusing circle. X-rays collected by the detectors are converted into electrical pulses that can be used to draw diagrams of the intensity of the diffracted radiation as a function of the diffraction angle:

$$I = f(2\theta) \qquad (I\text{-}1)$$

which is the basis of the analysis.

XRD analysis of ZnO thin films provides valuable insights into their crystal structure and phase purity, enabling researchers to understand and optimize film growth, characterize structural properties, and evaluate film quality. This information is crucial for various applications, including electronics, photonics, sensing, and energy devices where precise control over the thin film crystal structure is essential.

I.3.7.6 Bragg's Law

Bragg's law, named after Sir William Henry Bragg and his son Sir William Lawrence Bragg, is an essential law of X-ray diffraction that describes the relation between the angle of incidence of an X-ray beam and the distance between the planes of a crystal lattice. If one calculates the directions in which one has of the signal Figure I-16, one realizes that one obtains a very simple law, if one draws parallel imaginary planes passing by the atoms, and if we call the distance between these planes. This law can be expressed mathematically as:

$$2d\ sin\ (\theta) = n.\lambda \qquad (I\text{-}2)$$

Where:

n: Integer, diffraction order

d: Distance between the plans (hkl)

θ: Half-angle of deviation

λ: Wavelength of X-rays

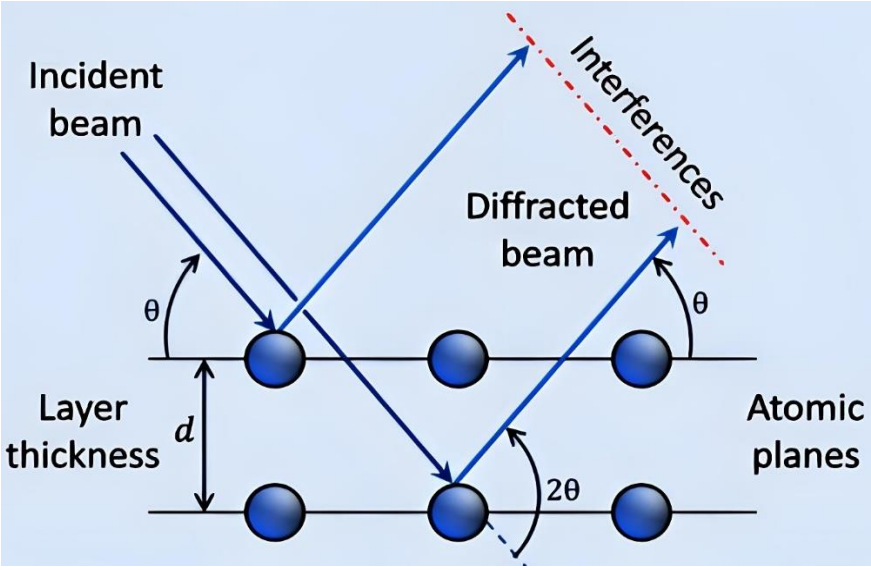


Figure I-16:Bragg's law giving the directions where the interferences are constructive.

Since the crystallographic planes can be identified by the Miller indices (hkl), the diffraction peaks can be indexed according to these indices. Thus, each material will be characterized by a series of peaks which correspond to the reflections due to its various atomic planes. The stripping is done using the cards (ASTM) containing the crystalline structure of each material with all the lines (depending on the angle θ) and their relative intensities [4].

I.3.7.7 Diffractometer

A diffractometer is a specialized instrument used for X-ray diffraction measurements, which is particularly useful for the characterization of thin films. A diffractometer consists of a sample holder, an X-ray source, and a detector. The sample holder can be rotated to change the orientation of the sample, while the X-ray source and detector remain fixed. In our study, we used a diffractometer of the type:

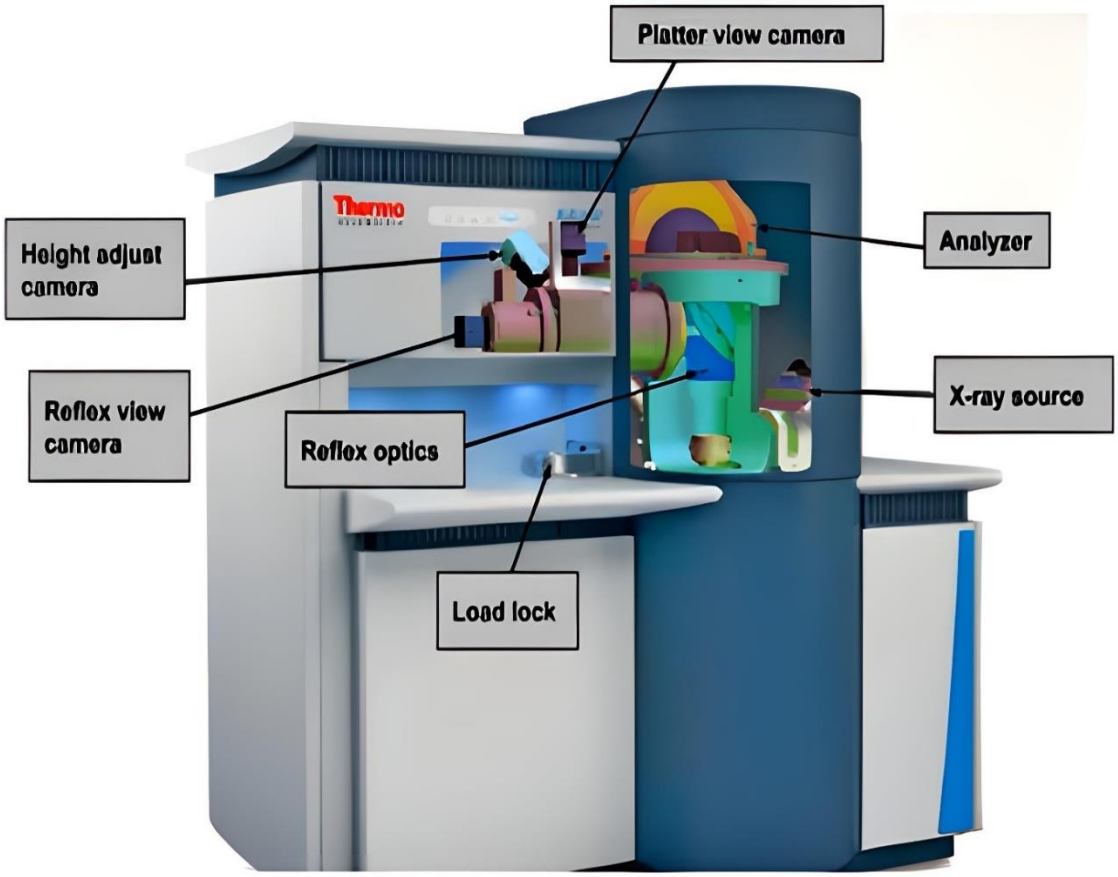


Figure I-17:Type diffractometer (Thermo K-Alpha monochromate high-performance XPS spectrometer).

There are several types of diffractometers, including:

1. Powder diffractometer: This type of diffractometer is used to analyze powder and polycrystalline materials. It usually uses a rotating sample holder to obtain a complete diffraction pattern in a short time.

2. Single crystal diffractometer: This category of diffractometer is used for the analysis of single crystals. Typically using a goniometer, he spots a crystal within an X-ray beam and collects diffraction data from multiple angles.

3. Small angle X-ray scattering (SAXS) diffractometer: This style of diffractometer is used to analyze the structure of materials at the nanoscale. It typically uses a collimated X-ray beam and a detector to measure scattered X-rays at small angles.

4. Small angle X-ray scattering (SAXS) diffractometer: This type of diffractometer is used to study the structure of materials at the nanoscale. It ordinarily uses a collimated X-ray beam and a detector to measure scattered X-rays at small angles.

5. Residual stress diffractometer: This type of diffractometer is used to analyze the residual stress present in a material. It typically uses goniometers and detectors to measure changes in lattice spacing due to residual stress in the material.

I.3.7.8 Determination of grain size and constraints

Grain size refers to the size distribution of grains or particles in a material, such as a metal or deposit. Determining the grain size of a material can provide important information about its properties, including strength, durability, and porosity. There are several methods for determining grain size, including:

1. Optical microscopy: This involves examining the material under a microscope and measuring the size of the grains using a calibrated eyepiece graticule. This technique is relatively simple and can be used for a wide range of materials.

2. X-ray diffraction: This involves analyzing the diffraction pattern of X-rays as they pass through the material, which can provide information about the crystal structure and grain size.

3. Electron microscopy: This involves using an electron microscope to examine the material at very high magnification, which can provide detailed information about the grain structure and size.

Constraints on grain size determination include the resolution of the equipment used and the sample preparation techniques employed. For example, if a sample is not properly prepared, it may be difficult to accurately measure the grain size. Additionally, different methods may be better suited for different types of materials or grain structures. It is also important to consider the statistical significance of any measurements taken, as grain size can vary significantly even within a small sample.

I.3.7.8.1 Determination of grain size

the size of grains in a material can be determined from the diffraction spectra obtained by X-ray diffraction (XRD) analysis. XRD is a powerful analytical technique that can provide information about the crystal structure, orientation, and grain size of a material. The diffraction pattern obtained from XRD analysis is a series of peaks that correspond to the scattering of X-rays by the crystal lattice of the material. The position and intensity of these peaks provide information about the crystal structure and orientation, while the width of the peaks is related to the size of the grains in the material. Using the Scherrer relation:

$$D = \frac{0.94\lambda}{\Delta\beta_{hkl}.cos\theta_{hkl}} \qquad (I\text{-}3)$$

Where:

D: the average size of the crystallites

β: the FWHM (the width at mid-height)

θ: the diffraction angle

λ: the wavelength of the Al Kα line.

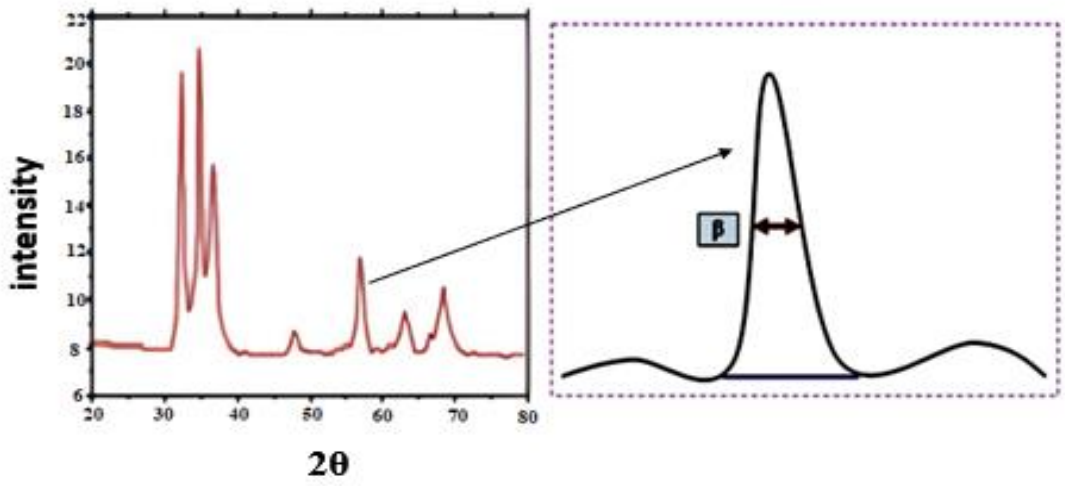


Figure I-18:Illustration showing the definition of β from the X-ray diffraction spectrum.

The Scherrer equation is a widely used method for estimating the grain size from the XRD data. This equation relates the width of a diffraction peak to the grain size and other factors such as the wavelength of the X-rays and the shape of the grains. By analyzing the width of the diffraction peaks in the XRD spectra, it is possible to estimate the average grain size of the material.

In the last, it is important to note that the grain size estimated by XRD analysis may not represent the actual grain size distribution in the material, as XRD provides an average value for the grain size. Other techniques such as electron microscopy may be needed to obtain a more detailed understanding of the grain size distribution in the material. General, XRD analysis is a powerful tool for determining the grain size of a material and can provide valuable information for understanding and optimizing its mechanical and physical properties.

I.3.7.8.2 Determination of constraints

The effect of the stresses in a material can be reflected in its X-ray diffraction pattern, also known as a diffractogram. This is because when a material is subjected to stress, it can cause changes in its crystal structure, which in turn affects the diffraction pattern of X-rays that pass through the material. One of the main ways that stress affects diffraction patterns is through the phenomenon of lattice strain. When a crystal is subject to stress, the distance between its lattice planes may change, leading to a shift in the position of the diffraction peaks in the diffractogram. This shift is proportional to the amount of stress in the material, and can be used to quantify the magnitude and direction of the stress. Additionally, stress can also cause changes in the intensity and width of the diffraction peaks in the diffractogram. This is because stress can cause defects or dislocations in the crystal lattice, which can affect the scattering of X-rays and lead to changes in the peak shape and intensity.

If the mesh parameter C0 (C0 = 5.205 A °) for an unstressed crystal becomes c for a constrained crystal, the internal stresses can be calculated from the following expressions:

$$\sigma = \left[2C_{13}.\frac{(C_{11}+C_{12}).C_{33}^{layer}}{C_{13}}\right]e_{zz} \qquad (I\text{-}4)$$

$$With: C_{33}^{layer} = \frac{0.99C_{33}^{cristal}}{(1-e_{zz})^4} \; and \; e_{zz} = \frac{C_0 - C}{C}$$

For the elastic constants C_{11}, C_{12}, C_{13} and C_{33} appearing in these formulas.

Overall, X-ray diffraction is a powerful tool for analyzing the crystal structure and stress state of materials, and can provide valuable information for understanding and optimizing their mechanical properties.

I.3.7.9 UV-Visible Spectroscopy

UV-Visible (UV-Vis) spectroscopy is a technique used to measure the absorption and transmission of light in the ultraviolet and visible regions of the electromagnetic spectrum. This technique is useful for characterizing thin films of materials like ZnO, which have strong optical properties in these regions. UV-Visible spectroscopy is a commonly used analytical technique that measures the absorbance or transmittance of light in the ultraviolet and visible regions of the electromagnetic spectrum. It is used to study the electronic structure and properties of materials, including molecules, ions, and solid-state materials.

In UV-Visible spectroscopy, a sample is exposed to light of a specific wavelength, and the amount of light absorbed or transmitted by the sample is measured. The amount of absorption or transmission depends on the electronic structure of the material, including the arrangement of its atoms and the energy levels of its electrons. UV-Visible spectroscopy is widely used in many fields, including chemistry, biology, physics, and materials science. Some common applications of UV-Visible spectroscopy include:

1. Determination of the concentration of a substance: UV-Visible spectroscopy can be used to determine the concentration of a substance in a sample, based on the amount of light absorbed by the sample at a specific wavelength.

2. Characterization of chromophores: Chromophores are groups of atoms within a molecule that are responsible for its color. UV-Visible spectroscopy can be used to identify and characterize chromophores in a molecule.

3. Analysis of electronic structure: UV-Visible spectroscopy can provide information about the electronic structure and properties of materials, including the energy levels and electronic transitions of their constituent atoms and molecules.

4. Study of reaction kinetics: UV-Visible spectroscopy can be used to monitor the progress of chemical reactions in real time, by measuring changes in absorbance or transmission over time.

UV-Vis spectroscopy is a useful technique for the characterization of ZnO thin films due to its simplicity, non-destructiveness, and ability to provide information on both the

electronic and optical properties of the film. It is commonly used in research and development of ZnO-based optoelectronic devices, such as solar cells, thin film transistors (TFTs), and photodetectors.

I.3.7.9.1 Operation the monochromator UV

The fields of spectroscopy are generally distinguished according to the wavelength range in which the measurements are made. The following areas can be distinguished: ultraviolet-visible, infrared and microwave. In our case, we used a dual-beam recording spectrophotometer, whose operating principle is shown in Figure I-19, by which we could draw curves representing the variation of the transmittance, depending on the length of the beam. Wave in the UV-Visible range (200-800 nm). Using these curves, it is possible to estimate the thickness of the film. And determine its optical characteristics; the optical absorption threshold, the absorption coefficient, the width of the forbidden band, the Urbach energy and the refractive index [56].

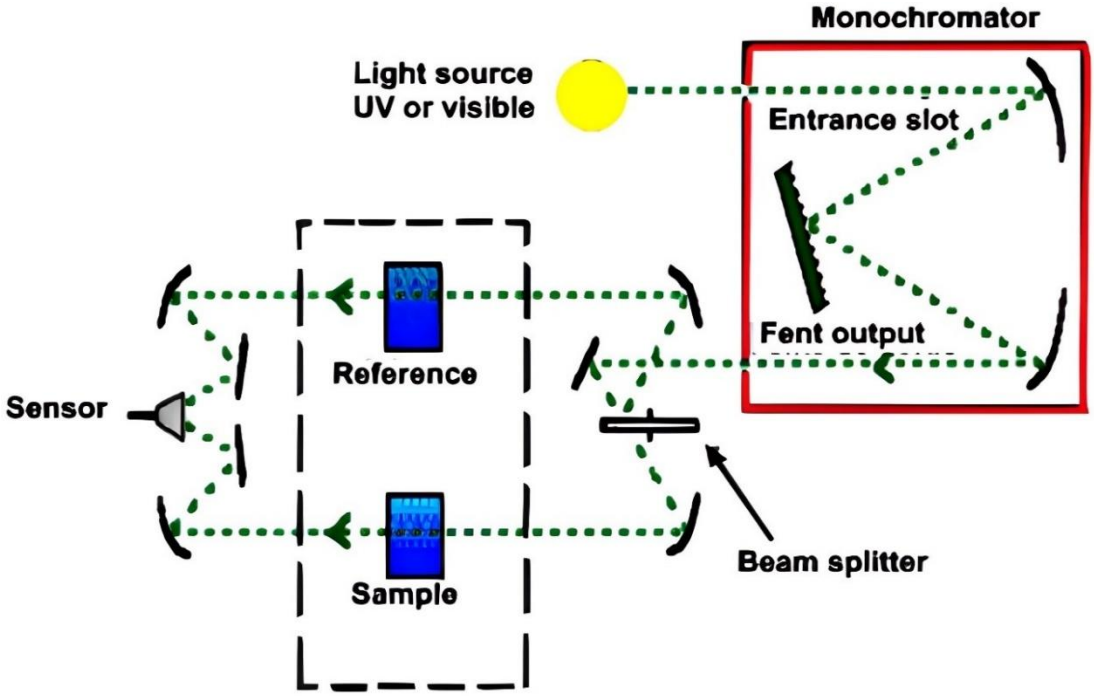


Figure I-19:Schematic representation of the UV-Visible spectrophotometer.

A monochromator is an optical device used in UV spectroscopy to isolate a specific wavelength of light from a source that emits a range of wavelengths. In UV spectroscopy, monochromators are typically used to select a specific wavelength of ultraviolet light from a

UV lamp or another source, which is then used to irradiate a sample.

Monochromators can be designed to operate in various modes, such as scanning mode or fixed wavelength mode. In scanning mode, the monochromator is used to sequentially isolate each wavelength in a range, which can then be used to generate a UV spectrum of the sample. In fixed wavelength mode, the monochromator is used to select a specific wavelength of light that is used to irradiate the sample for a specific purpose, such as a photolysis experiment. The choice of monochromator depends on various factors, including the desired wavelength range, resolution, and sensitivity. Different types of monochromators include prism monochromators, grating monochromators, and tunable filters.

I.3.7.9.2 The transmittance spectra

The transmission coefficient, or transmittance T, is defined as the ratio of the light intensity transmitted to the incident light intensity. To have the transmittance curves, our ZnO layers were deposited on the glass substrates. The latter is essential because it does not absorb light in the spectral domain studied. A blank substrate in the reference beam of the spectrophotometer, was used to plot the spectra, a computer connected to this device reproduces the spectra representing the transmittance, depending on the wavelength of the incident beam.

An example of these spectra is shown in Figure I-20, where we distinguish two domains:

A domain towards the longer wavelengths, where the transmittance presents a series of interference fringes due to multiple reflections in the ZnO layer. This area will allow us to determine the thickness of the layer and the refractive index. The second domain, where the transmittance begins to decrease rapidly, will be used for the determination of the optical absorption threshold.

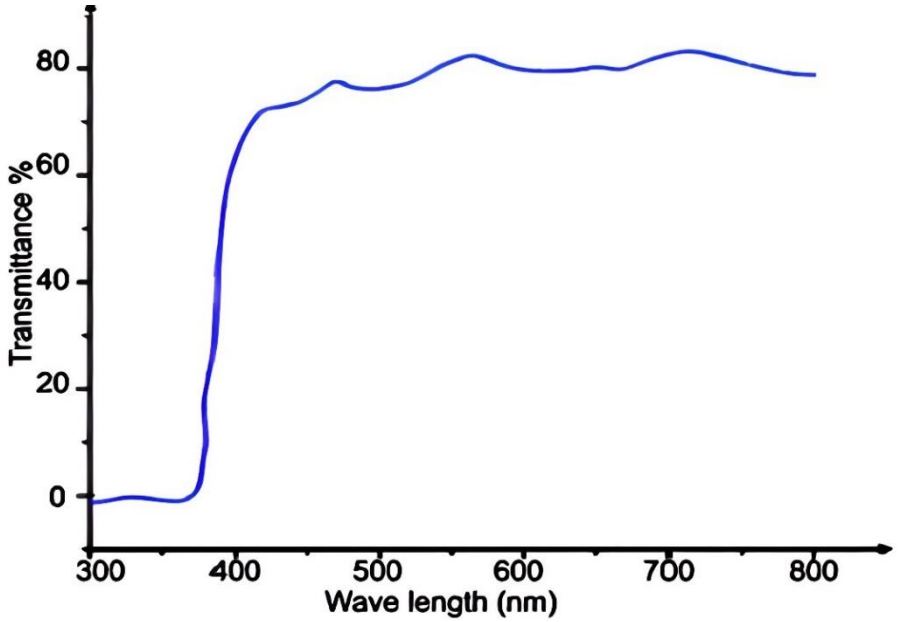


Figure I-20:Transmittance spectrum of ZnO as a function of wavelength [57].

A transmittance spectrum as a function of wavelength is a plot of the amount of light transmitted through a sample as a function of the wavelength of the light. In UV-Visible spectroscopy, this is typically shown as a graph with wavelength on the x-axis and transmittance or absorbance on the y-axis. The transmittance spectrum is obtained by passing a beam of light through the sample and measuring the amount of light that is transmitted through the sample as a function of the wavelength. The transmittance is defined as the ratio of the intensity of the transmitted light to the intensity of the incident light. Alternatively, the absorbance spectrum can be obtained by measuring the amount of light that is absorbed by the sample as a function of the wavelength. The absorbance is defined as the negative logarithm of the transmittance.

The transmittance spectrum can provide valuable information about the electronic and optical properties of the sample, including the presence of chromophores, the concentration of the sample, and the energy levels of the electrons in the sample. The shape and intensity of the spectrum can also provide information about the molecular structure of the sample and the interactions between the sample and the light.

I.3.7.9.3 Determination of the absorption coefficient

From the transmission spectrum of a layer one can calculate the absorption coefficient α and the extinction coefficient k of the material which constitutes it, using the Bouguer Lambert-Beer relation or often simply called; the law of Beer:

$$T = e^{-\alpha d} \quad (I\text{-}5)$$

If one expresses the transmittance T, in (%), the absorption coefficient is given by:

$$\alpha = \frac{1}{d} ln\ ln\ \left(\frac{100}{T(\%)}\right) \quad (I\text{-}6)$$

Where: d is the thickness of the coating and T is the transmittance.

It should be noted that this calculation implies that (1-T) is the absorption of the layer, whereas in fact part of the incident light is neither absorbed nor transmitted but is reflected. This approximation is all the less valid as the thickness of the layer is lower. We must therefore be very careful if we want to compare α for very different layer thicknesses.

The absorption coefficient provides information about the ability of the material to absorb light at a specific wavelength, and can be used to determine the concentration of the absorbing species in a sample. It can also be used to compare the absorption properties of different materials, and to study the electronic and optical properties of materials.

I.3.7.9.4 Determination of the band gap and Urbach energy

Zinc oxide (ZnO) is a semiconductor material that has a direct band gap. The band gap of ZnO is an important parameter that determines its electronic and optical properties. The band gap of ZnO can be determined experimentally using UV-Visible spectroscopy. In this method, the transmittance or absorbance spectrum of a thin film of ZnO is measured in the UV-Visible region of the electromagnetic spectrum. The band gap energy can be calculated from the onset of the absorption edge, which corresponds to the energy required to excite an electron from the valence band to the conduction band.

In the high absorption domain for a direct gap such as that of ZnO, α is expressed as a function of the gap (Eg) according to the following equation [58].

$$(\alpha h\nu) = A\left[h\nu - E_g\right]^{\frac{1}{2}} \quad (I\text{-}7)$$

A: constant.

E_g [eV]: optical gap.

$h\nu$ [eV]: the energy of a photon.

By scanning the entire energy domain, we have plotted $(\alpha h\nu)^2$ as a function of the energy of a photon E = $h\nu$ (knowing that) and that we extend the linear part of α^2 up to the axis abscissa (that is to say for $\alpha^2 = 0$), we obtain the value of E_g.

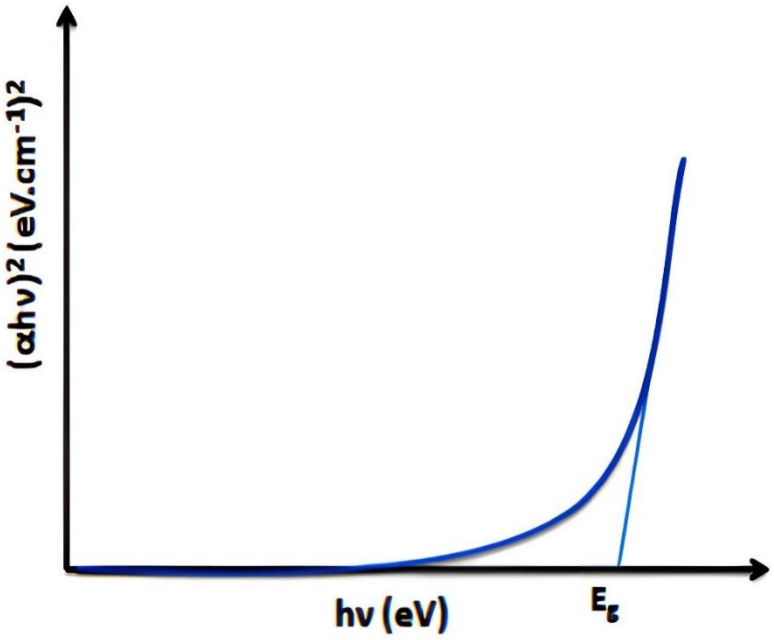


Figure I-21:Determination of gap energy by extrapolation from the variation of $(\alpha h\nu)^2$ versus $h\nu$ for a thin layer of ZnO.

The band gap energy of ZnO is typically in the range of 3.3 to 3.4 eV, depending on the crystal structure, doping, and other factors. The direct band gap nature of ZnO makes it an attractive material for various applications, including optoelectronics, solar cells, and photocatalysis. The band gap of ZnO can also be calculated theoretically using various computational methods, such as density functional theory (DFT). These methods can provide valuable insights into the electronic and optical properties of ZnO, and can be used to predict the behavior of ZnO under different conditions or in different applications.

Another important parameter that characterizes the disorder of the material is the Urbach's energy. Urbach energy is a parameter that characterizes the disorder and imperfections in the crystal structure of a material, particularly in semiconductors. It is named after the German physicist, Friedrich Urbach, who first proposed the concept in 1953[59].

In semiconductors, the bandgap energy represents the minimum amount of energy required to excite an electron from the valence band to the conduction band. However, in real materials, there are always defects and impurities that cause localized states within the bandgap.

These localized states have different energy levels that can trap electrons or holes, thereby affecting the electronic and optical properties of the material. According to Urbach's law the expression of the absorption coefficient is of the form [60]:

$$\alpha = \alpha_0 . exp\left(\frac{h\nu}{Eu}\right) \quad (I\text{-}8)$$

By plotting $ln\ ln\ (\alpha)$ according to $h\nu$, one can access the determination of the value of Eu or E_{00}:

$$ln\ ln\ (\alpha) = ln\ ln\ (\alpha_0) + \frac{h\nu}{Eu} \quad (I\text{-}9)$$

Eu can be estimated from the Figure I-20.
Ln(α) of ln(α) has in function of hv.

The Urbach energy (Eu) is a measure of the width of the distribution of localized states in the bandgap of a semiconductor. It is determined experimentally from the slope of the linear region of the exponential tail of the absorption edge in the UV-Vis absorption spectrum of the material. The Urbach energy is related to the density of states (DOS) of the material, with a smaller Urbach energy indicating a narrower distribution of localized states and a more ordered crystal structure. A higher Urbach energy indicates a broader distribution of localized states and a more disordered crystal structure. In general, a lower Urbach energy is desirable for semiconductor applications, as it indicates fewer defects and better electronic properties.

Chapter II: History and operation at the thin film transistors

Chapter II: History and operation at ZnO the thin film transistors

II.1 Introduction

The story of ZnO TFTs begins with the recognition of zinc oxide as a semiconductor material possessing intriguing properties. Despite its long history as a material of interest in fields such as optoelectronics and photocatalysis, ZnO's potential for TFT applications has gained prominence relatively recently. This interest was fueled by its high electron mobility, which rivals that of traditional TFT materials like silicon, as well as its transparency and compatibility with low-temperature deposition techniques.

The operation of ZnO TFTs revolves around the manipulation of charge carriers within thin films of zinc oxide. By modulating the electrical properties of these films through the application of gate voltages, TFTs can effectively control the flow of current between source and drain electrodes, enabling functionalities crucial for electronic devices. Understanding the mechanisms underlying ZnO TFT operation is essential for optimizing device performance and advancing the field of thin-film electronics.

II.2 Oxide Semiconductors and Oxide TFTs: History

Figure II-1 summarizes the history of oxide semiconductor and their TFTs. The research of oxide TFTs started in mid-1960s but had almost disappeared in open-accessible literatures after that until 1990s. The next oxide TFT reappeared in 1996 as an epitaxial SnO_2 TFT combined with a ferroelectric gate and became active in 2000s due to expectation that polycrystalline ZnO (poly-ZnO) can produce semiconductor active layers even at low temperatures including RT by keeping reasonable Hall mobilities >10cm^2 (V s)$^{-1}$[61]. This feature is considered to be very promising for low-temperature, large-area devices such as solar cells (SCs) and FPDs. Oxides are already used as transparent window electrodes and such oxides are called transparent conducting oxides (TCOs). However, active layers in semiconductor devices require low carrier density, low defect density, but satisfactory high mobilities; these kinds of materials are now called transparent oxide semiconductors (TOSs) instead of TCOs. As mentioned previously, good TCOs are required to improve devices such as SCs and FPDs because better transparency/electrical conductivity improves energy conversion efficiency in SCs and reduces power consumption and improves picture quality in

FPDs; on the other hand, good TOS active layers, for example, in TFTs, improve device size/resolution, electrical current drivability, operation speed, and so on and enable applications to next-generation LCDs and OLEDs. These applications are expanding to higher frame rates, 3D displays, flexible displays, and transparent displays.

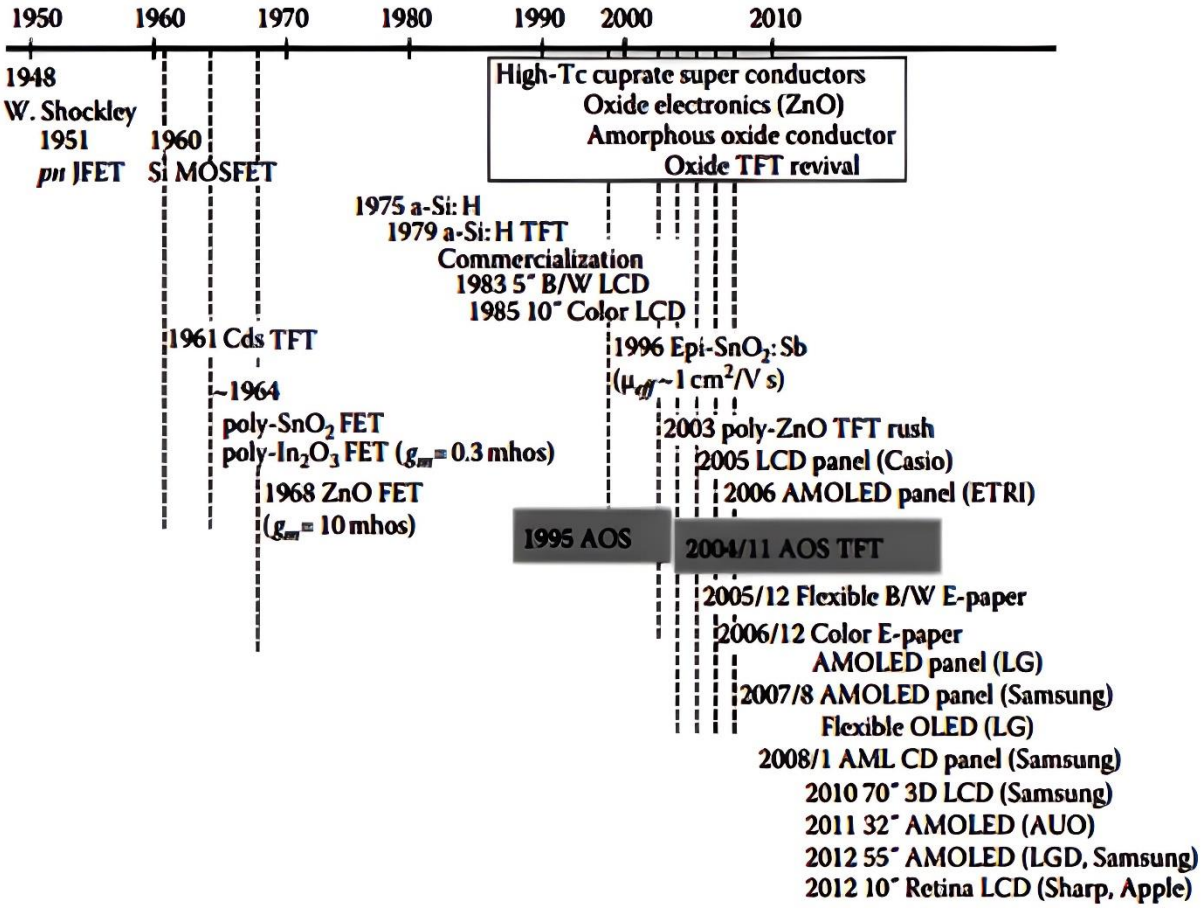


Figure II-1:History of oxide semiconductors and TFTs. [62].

The study of oxide thin-film transistors (TFTs) was initially limited to polycrystalline materials until the late 2004. However, polycrystalline n-type oxide semiconductors, specifically ZnO and SnO_2, exhibit sensitivity to environmental atmospheres due to the adsorption of oxygen-related species on their surface and grain boundaries (GBs). This adsorption process traps carrier electrons, while desorption induces a reverse effect. These properties, commonly observed in gas sensors, are intrinsic to n-type oxide semiconductors. The long-term stability, a significant hurdle for commercialization, also stems from the intrinsic characteristics of the surfaces and GBs in polycrystalline oxide semiconductors. Despite the initial expectation of using poly-ZnO as channel materials in TFTs, it has been discovered that

these materials still face challenges such as reduced mobility and stability, likely attributed to the issues associated with GBs [63].

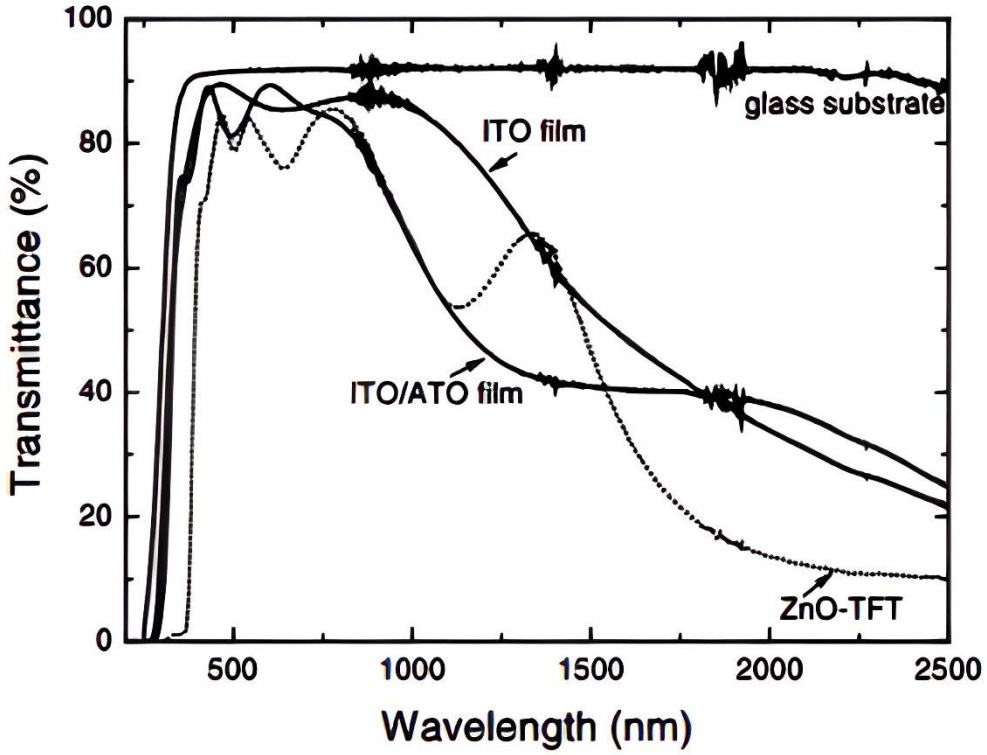


Figure II-2:Optical transmission spectra for the entire ZnO-TFT structure including the glass substrate.

It was observed that the ZnO thin-film transistor (TFT) exhibits complete transparency to visible light. In order to compare its optical transmission characteristics, the optical transmission spectra of the glass substrate (1.1 mm thickness), the indium tin oxide (ITO) film, and the ITO/ATO films are also included. The baseline and reference measurements were performed in air to determine the overall amount of transmitted light. The lower section of the study presents a photograph of a glass substrate measuring 2.5 × 2.5 cm^2, on which ZnO-based TFTs are placed [64].

II.3 Zinc oxide thin film transistors

Zinc oxide (ZnO) thin film transistors (TFTs) are electronic devices that employ thin films of ZnO as the active semiconductor layer. These TFTs have gained considerable interest in recent years due to their potential for high-performance and low-power electronic applications. Typically, ZnO TFTs consist of essential components such as a gate electrode, a dielectric layer, a ZnO thin film, and source and drain electrodes. The ZnO thin film functions

as the active semiconductor layer, while the gate electrode and dielectric layer control the current flow through the channel between the source and drain electrodes.

II.3.1 History of ZnO TFT

The history of ZnO TFTs (thin-film transistors) can be traced back to the early 1990s, when researchers first started investigating the use of ZnO as a transparent conducting oxide (TCO) material for optoelectronic applications[65]. At that time, indium tin oxide (ITO) was the dominant TCO material, but it was expensive and had limitations in terms of its transparency and electrical properties.

In 1995, a research group at the Tokyo Institute of Technology in Japan reported the first ZnO TFTs fabricated by sputtering ZnO thin films on a glass substrate[65]. These early ZnO TFTs had low mobility and on/off ratio, but they demonstrated the potential of ZnO as a TFT material. Over the next few years, researchers around the world continued to study ZnO TFTs, exploring different deposition methods, doping techniques, and device structures to improve their performance. In 2001, researchers at Penn State University in the US reported the first ZnO TFTs with high mobility and on/off ratio, using a pulsed laser deposition technique to fabricate the ZnO thin films[66]. Since then, ZnO TFTs have been the subject of extensive research, with a focus on improving their electrical and optical properties for various applications, such as displays, sensors, and photovoltaics. Some of the key developments in ZnO TFTs include the use of transparent conductive layers, such as ZnO-Al, for improved device performance, and the integration of ZnO TFTs with other electronic components, such as organic light-emitting diodes (OLEDs).

Today, ZnO TFTs continue to be an active area of research, with ongoing efforts to improve their performance and explore new applications.

II.3.2 Introduction

The thin film transistor (TFT) is a widely used transistor type in printed and flexible electronics. It derives its name from being constructed on thin films of materials, making it highly suitable for applications in printed electronics. TFT belongs to the category of Field-Effect Transistors (FETs), which regulate the flow of current between source and drain contacts by applying a voltage through the gate electrode. This voltage generates an electric field within the semiconductor, attracting and accumulating charges. As a result, a channel is formed that

facilitates the movement of charges between the source and drain contacts. Various semiconductor materials are employed in the fabrication of TFTs, each offering unique electrical and optical properties suitable for different applications in the field of electronics:

1. Amorphous Silicon (a-Si: H) and polycrystalline Silicon (Poly-Si) is the most common materials and are used in LCD screens and consumer electronics [67].
2. Zinc oxide and mixtures of ZnO (IZO, IGZO, ITZO… ex) [68].
3. Organic semiconductors: These are carbon-based materials that are used in organic TFTs (OTFTs). They offer flexibility and low-cost manufacturing compared to inorganic; it is different organic semiconductor material is used [69].
4. Other materials: There are many other semiconductor materials that can be used in TFTs, such as cadmium selenide (CdSe), and gallium arsenide (GaAs), among others. These materials are typically used in specialized applications or research settings [70].

II.3.3 Structure the ZnO TFT

ZnO has recently found other niche applications as well, such as fabrication of transparent thin-film transistors, where the protective covering preventing light exposure is eliminated since ZnO-based transistors are insensitive to visible light. Also, up to 2.10^{21} cm^{-3} charge carriers can be introduced by heavy substitutional doping into ZnO.

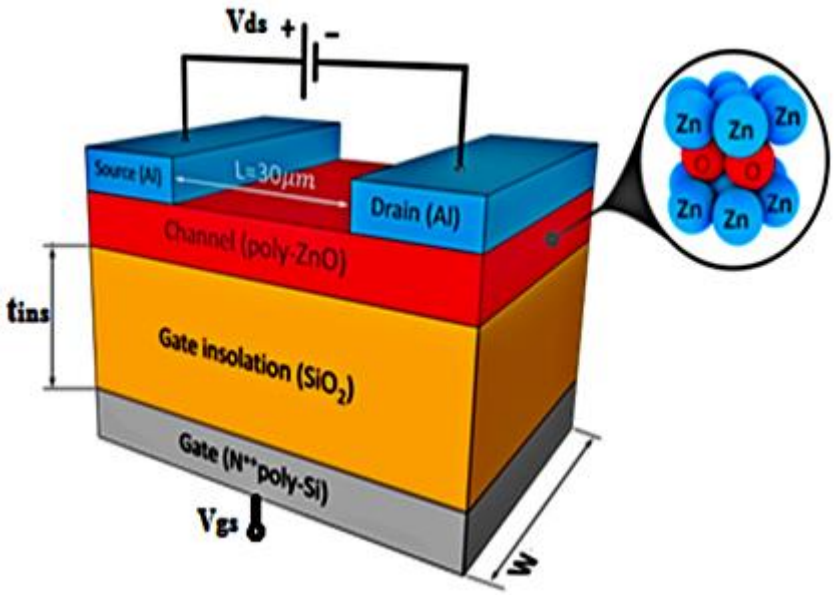


Figure II-3:ZnO-TFT schematic base structure used for the modeling.

Chapter II: History and operation at the thin film transistors

By controlling the doping level electrical properties can be changed from insulator through n-type semiconductor to metal while maintaining optical transparency that makes it useful for transparent electrodes in flat-panel displays [26].

Schematic base structure used for the modeling from top to bottom are:

1. Source and drain (metal contact): In a ZnO TFT (thin-film transistor), the source and drain are two depots that are used to control the flow of current through the device. The source is typically connected to a voltage drain, while the source is connected to the load. They are usually made of a strong conductive metal such as aluminum, silver or gold.

2. Channel the ZnO TFT: The channel in a ZnO TFT (thin-film transistor) is the region between the source and drain that is responsible for carrying the current when the device is in operation. The channel is typically made of a thin layer of ZnO semiconductor material that is deposited on a substrate. The properties of the ZnO channel, such as its thickness, morphology, and crystallinity, can have a significant impact on the performance of the ZnO TFT. For example, a thinner channel can result in a higher on-current, while a more crystalline channel can improve the electron mobility. To form the channel in a ZnO TFT, a thin film of ZnO is deposited on a substrate using a deposition technique such as sputtering or chemical vapor deposition (CVD)[71]. The thickness and uniformity of the ZnO film are critical parameters that need to be controlled to ensure a high-performance device. When a voltage is applied to the gate terminal of the ZnO TFT, an electric field is created in the channel between the source and drain. This electric field induces a charge carrier (electrons or holes) in the channel, allowing current to flow from the source to the drain.

3. Gate isolation: In a ZnO TFT (thin-film transistor), the gate isolation is a layer of insulating material that separates the gate electrode from the channel region of the transistor. The gate isolation is important because it prevents the gate electrode from directly contacting the channel, which would otherwise result in a short circuit and prevent the transistor from functioning properly. The gate isolation is typically made of a thin layer of insulating material, such as silicon

dioxide (SiO_2), silicon nitride (SiNx), or a high-k dielectric material [72]. The thickness and dielectric constant of the gate isolation layer are important parameters that can affect the performance of the transistor. For example, a thicker gate isolation layer can increase the voltage required to turn on the transistor, while a high-k dielectric material can increase the capacitance of the gate isolation layer, which can improve the performance of the transistor. The gate isolation layer is typically deposited on top of the channel region of the transistor using a deposition technique such as sputtering, chemical vapor deposition (CVD), or atomic layer deposition (ALD). The gate electrode is then deposited on top of the gate isolation layer, and a metal contact is made to provide electrical contact to the gate electrode.

4. Gate electrode: In a ZnO TFT (thin-film transistor), the gate is a terminal that is used to control the flow of current through the device. The gate is typically made of a metal electrode, such as aluminum or gold, that is separated from the ZnO channel by a gate insulator material, such as silicon dioxide (SiO_2), silicon nitride (SiNx), or a high-k dielectric material. When a voltage is applied to the gate electrode, an electric field is created in the channel region of the ZnO TFT. This electric field controls the flow of charge carriers (electrons or holes) in the channel, allowing current to flow from the source to the drain.

II.4 The principal operation electrical characteristic of a TFT

The fundamental operational characteristic of a Thin Film Transistor (TFT) is its capability to regulate the flow of electric current between two terminals. This control is achieved through the utilization of a thin film of semiconductor material, known as the channel, positioned between two electrodes, namely the source and drain. Commonly employed semiconductor materials for TFTs include oxides like zinc oxide (ZnO) or polysilicon layers. The electrodes, on the other hand, are typically composed of metals such as aluminum or copper. When a voltage is applied to the TFT, the thin film of semiconductor material functions as a switch, enabling the passage of current between the source and drain electrodes. This current can then be utilized to govern the flow of electrical current between the two terminals. The amount of current that can be controlled is determined by the thickness of the semiconductor material and the voltage applied to the TFT. Leveraging the electrical properties

of TFTs, an array of electronic devices can be developed, including displays, sensors, and memory chips.

The important parameters for a TFT (thin-film transistor) depend on the specific application and performance requirements, but generally include the following:

1. Drain current (I_d): The drain current is a measure of the electrical current flowing between the source and drain electrodes when a voltage is applied to the gate electrode. The drain current is an important electrical characteristic of the TFT, as it determines the amount of current that can be switched on and off by the device.
2. Field effect mobility (effective mobility of device) (μeff): Field effect mobility is a measure of the rate at which charge carriers move through the channel of a thin-film transistor (TFT) in response to an electric field applied by the gate electrode. It is an important electrical characteristic of TFTs, as it determines how quickly the device can switch on and off and how efficiently it can conduct electrical current.
3. Threshold voltage (V_{th}): The threshold voltage is the gate voltage required to turn on the TFT. This parameter is important for determining the operating range of the device.
4. Subthreshold slope (SS): This is a measure of the sensitivity of the TFT to changes in the gate voltage when the device is operating in the subthreshold region. A lower subthreshold swing is desirable for achieving faster switching and lower power consumption.
5. On/Off current ratio: The on/off ratio of the TFT is a measure of its ability to switch current on and off. Higher on/off ratios are desirable for many applications.
6. Contact resistance: This is the resistance at the interface between the channel and the source/drain electrodes. Low contact resistance is important for achieving efficient charge carrier injection and extraction, and for minimizing power consumption.
7. Capacitance: The capacitance of a TFT is the ability of the device to store electrical charge, and is determined by the capacitance of the gate dielectric layer and the area of the channel. The gate capacitance is typically much larger than the channel capacitance, and is a function of the dielectric constant of the gate dielectric material and the thickness of the dielectric layer.

8. Frequency response: The frequency response of a TFT refers to the ability of the device to respond to changes in the gate voltage at different frequencies. This is determined by the RC time constant of the device, which is a function of the capacitance of the gate dielectric layer and the resistance of the channel material[73]. At high frequencies, the RC time constant limits the ability of the device to respond to changes in the gate voltage, resulting in reduced switching speeds and poorer device performance.
9. Stability: The stability of TFTs is an important consideration, as the performance of the device can degrade over time due to various factors such as bias stress, temperature, and humidity.
10. Uniformity: This refers to the ability of the TFT to maintain its performance characteristics over time and under various operating conditions. Stability is critical for ensuring reliable device operation over the lifetime of the application.
11. Channel length and width (L,W): The channel length and width of a TFT determine the amount of current that can flow through the device. Smaller channel dimensions can lead to higher current density and faster switching times, but they can also increase the resistance of the device and reduce its overall performance.
12. Channel material and doping: The material used for the TFT channel, such as amorphous silicon, metal oxides (e.g. ZnO), or organic semiconductors, can significantly impact the device performance. Doping the channel material with impurities can also improve its conductivity and mobility.
13. Gate dielectric material: The gate dielectric material affects the capacitance of the TFT and determines the amount of charge required to switch the device on and off. High-k dielectric materials, such as hafnium oxide or aluminum oxide, can improve the device performance by reducing the voltage required to operate the device.
14. Gate electrode material: The gate electrode material affects the work function of the device and can impact the threshold voltage and switching speed of the device. Materials such as aluminum, gold, or platinum are commonly used for gate electrodes.
15. Source and drain electrode material: The source and drain electrodes are responsible for injecting and collecting charge carriers in the TFT. Materials such as aluminum, gold, or silver are commonly used for these electrodes.

Optimizing these parameters requires careful design and fabrication of the TFT, including selection of materials, device architecture, and processing conditions.

Thin-film transistors (TFTs) are typically biased by applying a voltage to the gate electrode, which controls the flow of current between the source and drain electrodes through the channel region. The gate voltage is typically negative in the case of n-type TFTs, which have an n-type channel material such as amorphous silicon or zinc oxide [74].

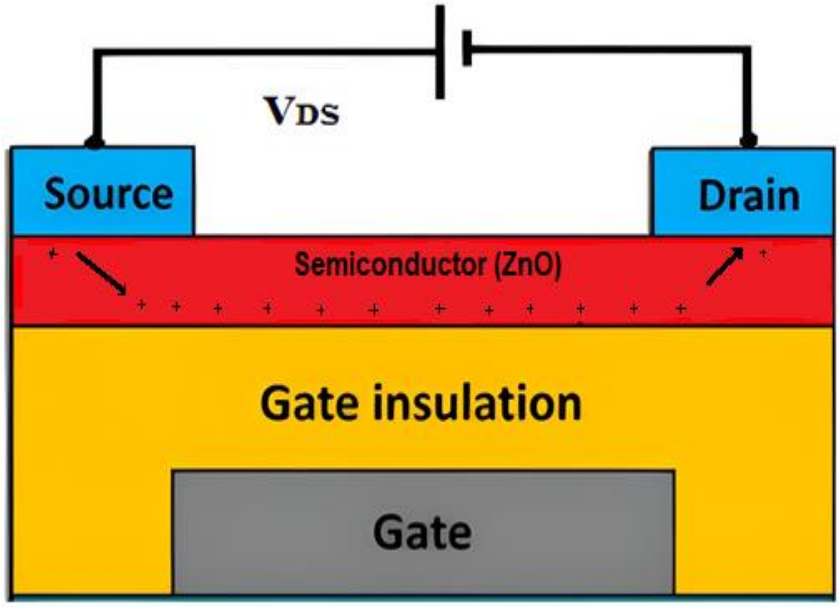


Figure II-4:Schematic TFT on a negative bias voltage.

The transistor remains in an off state, preventing the accumulation of charge between the source and drain contacts. Consequently, the flow of current between the source and drain is minimal or non-existent. To activate the transistor, a negative voltage bias, V_{DS}, is applied to the gate. This causes carriers (specifically, holes) in the semiconductor to accumulate near the gate insulation, leading to the formation of a channel that enables the current, I_{DS}, to flow from the drain to the source

II.4.1 Top gate ZnO TFTs

Top gate zinc oxide (ZnO) thin-film transistors (TFTs) are a type of TFT in which the gate electrode is located on top of the channel material and separated from it by a gate dielectric layer. Variation is to have the source and drain contacts deposited on top of the active layer (left) or directly on the substrate (right).

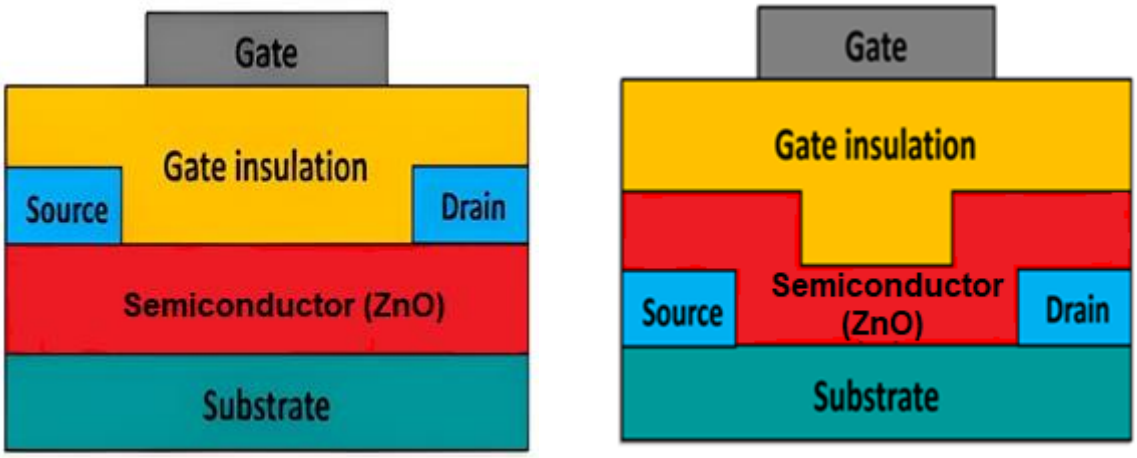


Figure II-5:Top gate ZnO-TFTs structures.

Top-gate ZnO TFTs offer various advantages in comparison to alternative TFT types. These advantages encompass enhanced regulation of the gate dielectric properties, streamlined fabrication procedures, and compatibility with flexible substrates. Nevertheless, top-gate ZnO TFTs also exhibit certain limitations, including elevated gate capacitance and a higher susceptibility to gate leakage currents when compared to bottom gate TFTs.

II.4.2 Bottom gate ZnO TFTs

Bottom gate ZnO TFTs have the gate contacts and insulator deposited first on the substrate and then the active layer. Variations are to deposit source and drain contacts on top of active layer (left) or top of the insulator. This is called top contact and bottom contact (not to be confused with top and bottom gate).

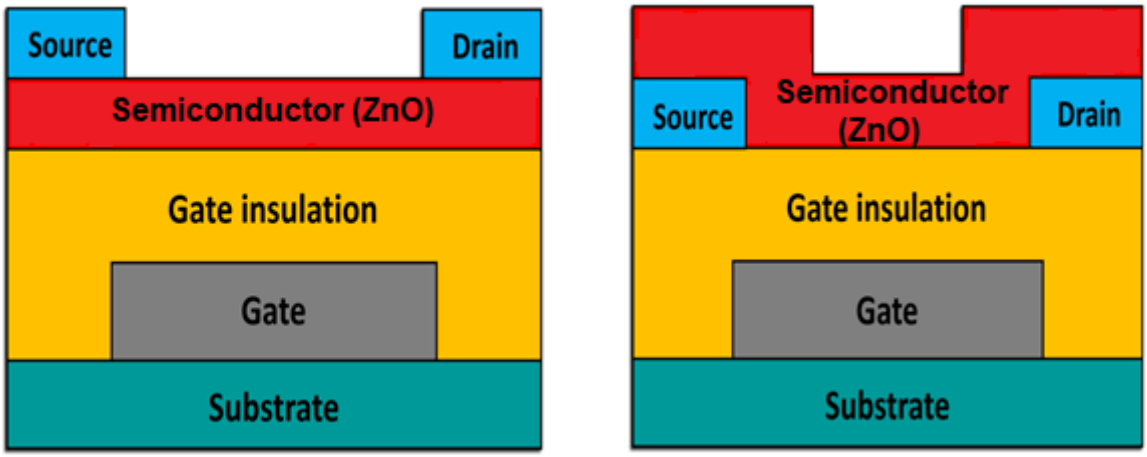


Figure II-6:Bottom gate ZnO-TFTs structures.

Bottom gate ZnO TFTs have several advantages over top gate TFTs, including lower gate capacitance, improved gate dielectric properties, and better control over the channel material properties. However, they also have some limitations, such as more complex fabrication processes and lower compatibility with flexible substrates.

II.4.3 Definition of ZnO transistor Size (W, L)

The size of a zinc oxide (ZnO) transistor refers to the dimensions of the transistor's channel, which is the region between the source and drain electrodes where the current flows. The channel size is typically specified by two parameters: the channel width (W) and the channel length (L).

The channel width refers to the distance between the source and drain electrodes along the direction perpendicular to the current flow. The channel length refers to the distance between the source and drain electrodes along the direction of the current flow.

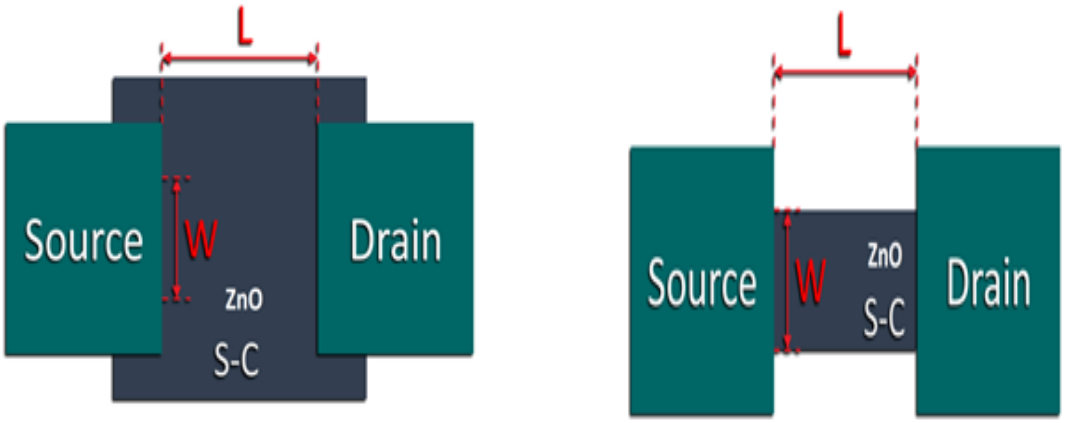


Figure II-7:Two dimensional ZnO-TFTs structures show (W, L).

The size of the transistor's channel, which refers to its dimensions, plays a crucial role in determining its electrical characteristics, such as drain current, field effect mobility, and switching speed. Typically, smaller channel dimensions lead to faster switching speeds and improved performance. However, achieving these benefits necessitates more precise fabrication techniques, and there is a greater susceptibility to variations and reliability concerns.

II.5 Operations of TFTs

The operations of a TFT are rooted in the principle of a field effect transistor (FET), where the manipulation of the electric field within a semiconductor channel is governed by the voltage applied to the gate electrode. By applying a voltage to the gate electrode, an electric field emerges within the semiconductor material, exerting attractive or repulsive forces on charge carriers, depending on the transistor type. Consequently, the conductivity of the semiconductor channel undergoes modification, consequently influencing the current that traverses between the source and drain electrodes.

For TFTs biased with a small voltage between the drain and the source the drain current (I_D) varies linearly with drain-source voltage (V_{DS}) and the channel has the characteristic of a resistor, it gives:

$$I_D = g_D . V_{DS} \qquad (II\text{-}1)$$

Where g_D is defined as the drain conductance.

The channel conductance is given as:

$$G_o = \frac{w}{L\ \mu\ |Q|} \qquad \textit{(II-2)}$$

Where w is the transistor channel width, and L is the transistor channel length, μ is the field effect mobility of the charge carriers in the channel; Q is the magnitude of the sheet density of the accumulated layer charge and is a function of gate-source voltage (V_{GS}) and the capacitance per unit area of the gate insulator C_i.

In the absence of traps, the accumulated layer charge is given as:

$$|Q| = C_i(V_{GS} - V_{th}) \qquad \textit{(II-3)}$$

Where V_{th} is threshold voltage and Ci the capacitance per unit area, given by:

$$C_i = \frac{\varepsilon.\varepsilon_0}{t_i} \qquad \textit{(II-4)}$$

Were ε_0 is the permittivity of free space. ε is the relative permittivity of the gate insulator and t_i it is the thickness of the gate insulator.

The performance of a TFT is typically characterized by its drain current, field effect mobility, and threshold voltage. The drain current is the current flowing between the source and drain electrodes when a voltage is applied to the gate electrode, and is a measure of the transistor's overall current-carrying capacity. The field effect mobility is a measure of the speed at which charge carriers move through the channel in response to the electric field created by the gate voltage. The threshold voltage is the voltage required to turn the transistor on, and is typically determined by the properties of the gate dielectric and the semiconductor material.

II.5.1 Field Effect Mobility

Field Effect Mobility in TFT (Thin Film Transistor) is a measure of how quickly electrons can move through a semiconductor material when an electric field is applied to it. It is an important parameter for determining the performance of a Thin Film Transistor (TFT) device. The mobility of electrons in a TFT is determined by the material properties of the semiconductor, such as its band gap, electron affinity, and doping concentration. The mobility of electrons in a TFT is typically measured in cm^2/Vs.

The mobility of electrons in a TFT is affected by several factors, such as temperature, electric field, and the type of semiconductor material used. As the temperature increases, the mobility of electrons in a TFT increases [75]. This is because the thermal energy of the electrons increases, allowing them to move more quickly through the semiconductor material. The electric field applied to the TFT also affects the mobility of electrons. A higher electric field will cause the electrons to move more quickly through the semiconductor material.

Field effect mobility is of crucial importance and a metric and process for semiconductor A higher mobility means:

1. A higher cutoff frequency.
2. A higher current can be passed.

The mobility relates the drain current I_{DS} to the drain and gate voltages (V_{DS}, V_{GS}), the threshold voltage (Vth) and the channel width and length (W, L). In the beginning of organic semiconductor mobilities were in the order of $\mu = 10^{-6}$ to 10^{-3} cm^2/Vs but now significant improvements give mobilities of $\mu = 0.01 - 0.1$ cm^2/Vs and even >1 cm^2/Vs[76]. Amorphous silicon a-Si μ~1 cm^2/Vs [77]. Polycristalline Silicon (Poly Si) μ~170 cm^2/Vs [78].

The mobility of electrons in a TFT is an important parameter for determining the performance of the device. A higher mobility of electrons in a TFT will result in a faster switching speed and a higher current density. This will result in a better performance of the device.

II.5.2 Linear operation the drain current

In the linear region of the transistor operation, when $V_{DS} < V_{GS} - V_{th}$ (meaning when the bias voltage applied to the gate minus the threshold voltage is larger than the voltage applied between source and drain) the following expression is used to describe the drain current Id:

$$I_{DS} = \frac{W\mu C_i}{2L}[2(V_{GS} - V_{th})V_{DS} - V_{DS}^2] \qquad (II\text{-}5)$$

For small $V_{DS}, V_{DS} << (V_{GS} - V_{th})$, this can be simplified to:

$$I_d = \frac{W\mu C_i}{L}(V_{GS} - V_{th})V_{DS} \qquad (II\text{-}6)$$

This equation represents the linear region of operation for a TFT, where the gate voltage is small enough that the transistor is not fully turned on. In this region, the drain current

increases linearly with the gate voltage, and the slope of the current-voltage (I-V) curve is determined by the device parameters such as the mobility and channel dimensions.

It is important to note that the linear region of operation is limited by the maximum drain voltage that the TFT can withstand without breakdown, which is typically around 15-30 volts for pc ZnO TFTs. Beyond this voltage, the TFT enters the saturation region, where the drain current levels off and becomes independent of the gate voltage.

II.5.2.1 Saturation region drain current

For a large drain to source voltage $V_{DS}>(V_{GS}-V_{th})$ and $V_{GS}>V_{th}$ the transistor is biased in the saturation region of operation. In this case because of the high V_{DS} voltage V_{GS} is reduced at the drain end of the channel and therefore the channel depth decreases to almost zero, so called pinch off.

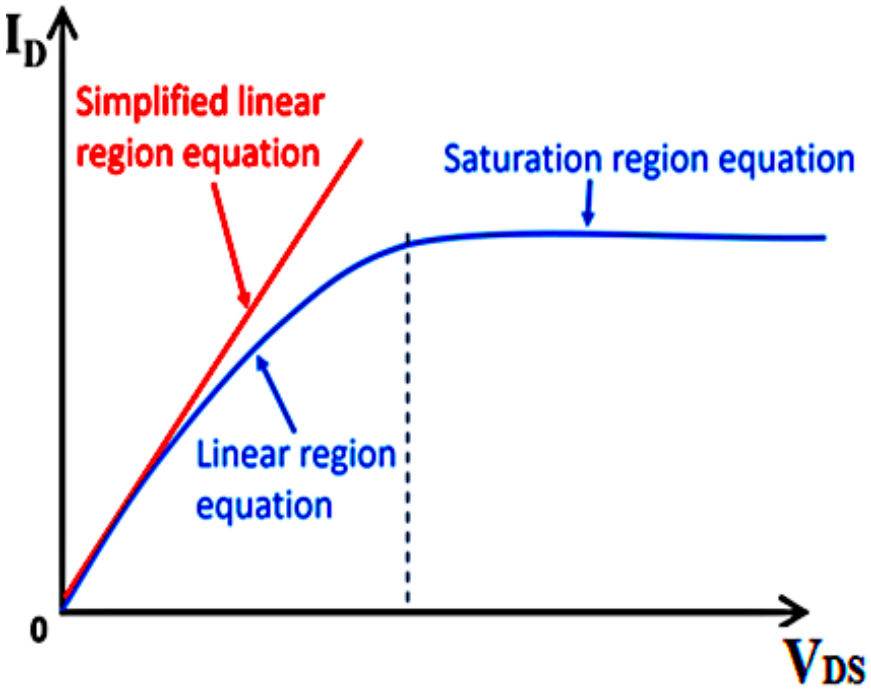


Figure II-8:Transfer characteristics $I_D=f(V_{DS})$ of the ZnO-TFT.

In this region, the transistor is fully turned on and the current is limited by the channel resistance and the applied drain-source voltage (V_{DS}) and the drain current is limited by the mobility of the electrons in the channel and the electric field in the channel region. The mobility determines how easily electrons can move through the channel, while the electric field determines how much the electrons are accelerated by the applied voltage.

When V_{gs} is increased in this case it will have very little effect, the current varies as the square of the gate source voltage and therefore the drain current Id saturates.

The saturation drain current can be obtained by replacement of $V_{DS} = V_{GS} - V_{th}$ into equation (II-.6).

This is shown in the following expression [79]:

$$I_{DS} = \frac{W\mu C_i}{2L}(V_{GS} - V_{th})^2 \qquad (II\text{-}7)$$

By controlling the parameters in the drain current equation, such as the gate voltage, channel length and width, and effective carrier mobility, the saturation region of a TFT can be engineered to achieve desired performance characteristics, such as high on-state current, low off-state leakage, and good linearity. Understanding and optimizing the saturation region behavior is essential for designing TFT-based devices.

II.5.2.2 Field effect mobility in linear region

The mobility, or field effect mobility (μ_{FE}) is different from the linear and saturation regions. In the linear region of device operation ($V_{DS}<V_{GS}-V_{th}$) the mobility is generally extracted from the transconductance of the device (g_m) which is the change in Id with V_{GS} for small and constant values of V_{DS}. This is given by:

$$g_m = \frac{\Delta I_d}{\Delta V_{GS}} = \frac{w\mu C_i}{L} V_{DS} \qquad (II\text{-}8)$$

Rearranging and solving for mobility gives:

$$\mu = \frac{g_m L}{W C_i}\left(\frac{1}{V_{DS}}\right) \qquad (II\text{-}9)$$

which is valid for small and constant V_{DS}.

In the linear region of operation, where the transistor is not fully turned on, the field effect mobility is relatively constant and is determined by the intrinsic properties of the semiconductor material and the quality of the film [80]. However, in the saturation region, the field effect mobility is affected by the channel-length modulation, which results in a decrease in the effective channel length at the drain end of the channel due to the electric field-induced reduction in the depletion layer width.

Therefore, the field effect mobility in the linear region is an important parameter that determines the overall performance of TFTs, and is typically characterized experimentally using various electrical measurement techniques, such as the transfer curve measurement and the four-point probe technique.

II.5.2.3 Extracting Field effect mobility in the linear region

In thin-film transistors (TFTs), the field effect mobility in the linear region is an important parameter that characterizes the ability of the transistor to conduct current under the influence of an electric field. The field effect mobility is defined as the ratio of the average drift velocity of the electrons in the channel to the electric field strength.

By plotting measured $I_{DS} - V_{GS}$ in the graph it is possible to extract the transconductance gm by fitting a line to $I_{DS} - V_{GS}$ above threshold and extracting the slope of the fitted line.

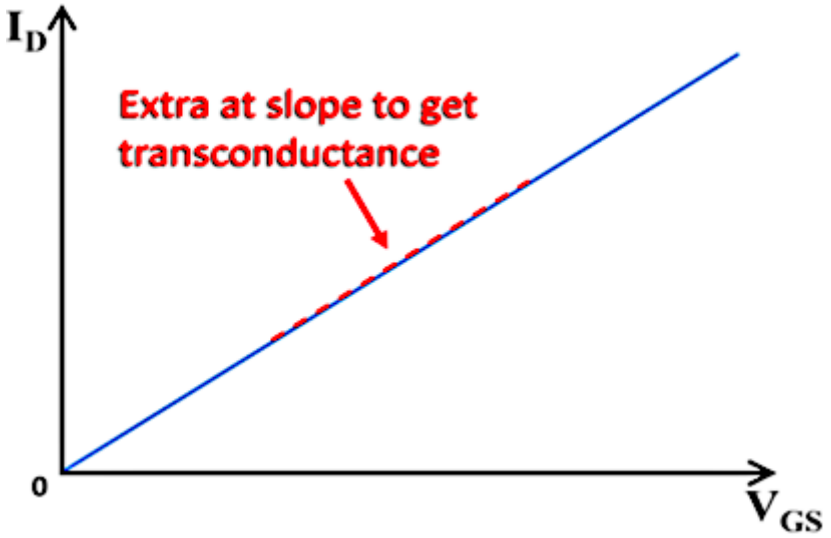


Figure II-9:Transfer characteristics I_{DS}=f(V_{GS}) of the ZnO-TFT.

The definition of transconductance is the ratio of the current variation at the output to the voltage at the input ($\Delta I/\Delta V$). The equation for mobility in the linear region is:

$$\mu = \frac{g_m L}{W C_i}\left(\frac{1}{V_{DS}}\right) \qquad (II\text{-}10)$$

So, by extracting transconductance and knowing the other parameters (W, L and C_i), the field effect mobility μ can then be extracted.

It is important to note that the field-effect mobility in the linear region of operation may not be the same as the bulk mobility of the semiconductor material. This is because the effective mobility in the channel is affected by various factors such as the scattering of electrons at the interface and the presence of defects and impurities in the semiconductor material.

II.5.2.4 Threshold Voltage

Threshold voltage (Vth) is a critical parameter in thin-film transistors (TFTs). It is the voltage at which the transistor starts to conduct current. It is an important parameter because it affects the performance of the transistor, such as its switching speed, power consumption, and leakage current [81]. The threshold voltage of a TFT is determined by the device structure, such as the channel length, channel width, and doping concentration. The doping concentration affects the threshold voltage because it determines the amount of charge carriers in the channel. The channel length and width affect the threshold voltage because they determine the resistance of the channel.

Also, threshold voltage can be extracted by extracting the line to zero drain current and locating the intercept with V_{GS}.

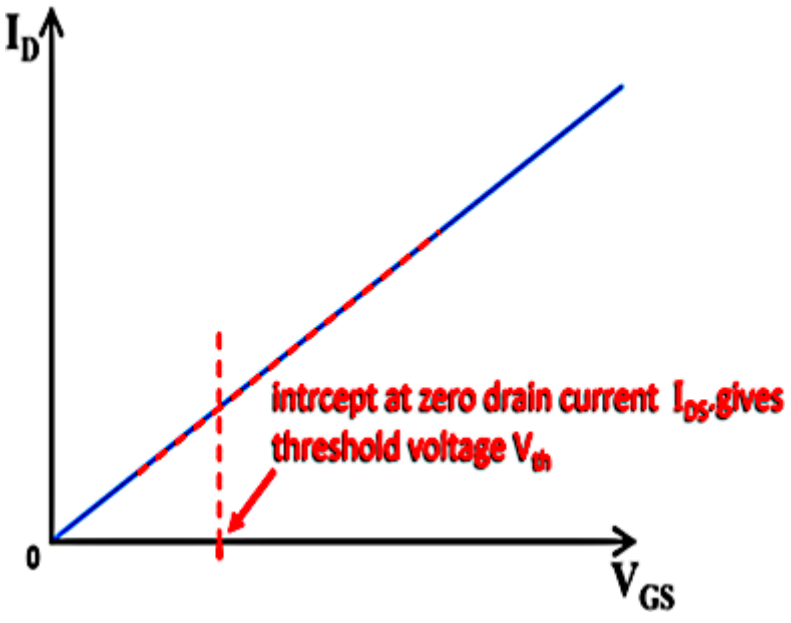


Figure II-10:Transfer characteristics $I_{DS}=f(V_{GS})$ of the ZnO-TFT in linear.

The threshold voltage in ZnO TFTs is typically very large and uncontrolled, reaching values of twenty volts. This is not generally understood, but can be an effect of a high density of trapped charge in the highly defective organic S-C [82].

In practice, the threshold voltage can be measured experimentally by measuring the drain current as a function of gate voltage and determining the gate voltage at which the current begins to increase. The threshold voltage is an important parameter in the design and operation of TFTs as it determines the voltage required to turn the transistor on and off, and thus affects the device performance and power consumption.

In summary, the threshold voltage of a TFT is determined by the device structure, such as the channel length, channel width, and doping concentration, as well as the gate voltage and temperature. Likewise, it is an important parameter in many applications of TFTs, such as in active-matrix displays and digital circuits. A precise control of the threshold voltage is required to achieve reliable and stable device operation.

II.5.2.5 Extracting field effect mobility in the saturation region

Field effect mobility in the saturation region of a thin-film transistor (TFT) is a measure of the transistor's ability to control current flow. It is defined as the ratio of the drain current to the gate voltage, and is usually expressed in units of cm^2/Vs [81]. The field effect mobility in the saturation region is determined by the properties of the semiconductor material used in the TFT

in the saturation region the field effect mobility is described by:

$$\mu = \frac{2L}{WC_i}\left(\frac{\Delta\sqrt{I_{DS}}}{\Delta V_{GS}}\right)^2 \qquad (II\text{-}11)$$

It can be extracted by fitting a line to $\sqrt{I_{DS}} - V_{GS}$ and extracting the slope.

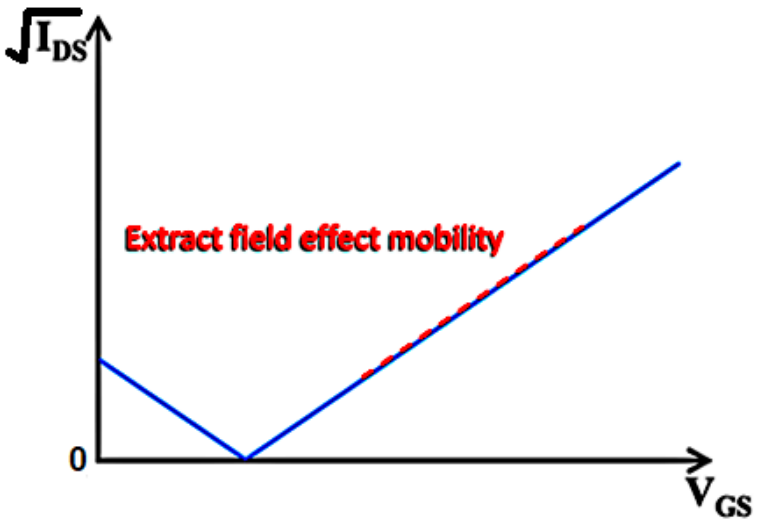


Figure II-11:Transfer characteristics $\sqrt{I_{DS}}$=f(V_{GS}) of the ZnO-TFT in saturation.

By knowing the other parameters, (W, L and C_i), the field effect mobility μ can be extracted from the expression. Moreover, the threshold voltage V_{th} can be extracted interpolating the fitted line down to the V_{GS} intercept at zero I_D.

In experimental test is the field effect mobility in the saturation region is typically measured using a four-point probe technique [83]. The four-point probe consists of two probes to measure the drain current and two probes to measure the gate voltage. The four-point probe is connected to a source-measurement unit (SMU) which is used to apply a voltage to the gate and measure the resulting drain current. The field effect mobility is then calculated from the ratio of the drain current to the gate voltage.

The field effect mobility in the saturation region of a TFT can be extracted using a four-point probe technique, a two-point probe technique, or by calculating the transconductance or on-state resistance. The field effect mobility is a measure of the transistor's ability to control current flow, and is expressed in units of cm^2/Vs.

II.5.2.6 *On/Off* current ratio

The on/off current ratio in TFT (Thin Film Transistor) is a measure of the performance of a TFT display. It is the ratio of the current flowing through the TFT when it is in the "on" state to the current flowing through the TFT when it is in the "off" state [84]. The higher the ratio, the better the performance of the display. The on/off current ratio is an important parameter for TFT displays because it determines the contrast ratio of the display. The contrast ratio is the ratio of the brightest white to the darkest black that the display can produce. A higher on/off current ratio means that the display can produce a higher contrast ratio.

The *On/Off* current ratio (I_{on}/I_{off}) is defined as the ratio of the current to the leakage current.
The *On/Off* current ratio is extracted from the $I_{DS} - V_{GS}$ characteristic plotted on a semilog scale.

The on/off current ratio is a critical factor in determining the power consumption of a display. A higher on/off current ratio indicates that the display consumes less power when it is in the "on" state. This is due to the reduced current flow through the thin-film transistor (TFT)

when it is in the "off" state. The on/off current ratio typically ranges from 10:1 to 1000:1 in TFT displays, with the specific ratio influenced by the type of TFT and the display's design. Generally, higher-quality TFTs exhibit higher on/off current ratios, contributing to improved energy efficiency and reduced power consumption in the display.

II.5.2.7 Subthreshold slope

Subthreshold slope (SS) in TFT is a measure of the steepness of the transistor's current-voltage (I-V) curve in the subthreshold region. The subthreshold region is the region of operation of a transistor where the current is below the threshold voltage (Vth). The subthreshold slope is a measure of the transistor's ability to control its current in the subthreshold region. It is usually expressed as the ratio of the change in current (ΔI) to the change in voltage (ΔV) in the subthreshold region [85]. The subthreshold slope of a TFT is determined by the device's physical structure and materials. It is typically measured in millivolts per decade (mV/decade) and is an important parameter for the design of low-power circuits. A lower subthreshold slope indicates that the transistor is more efficient in controlling its current in the subthreshold region, resulting in lower power consumption.
The standard equation for drain current in the subthreshold region is:

$$I_{DS} = \frac{W}{L} K \mu_{FE} C_{ox} \left(1 - e^{-qV_{DS}/nkT}\right) \qquad (II\text{-}12)$$

Has *K* been a constant that depends on the materials and device structure, n is the ideality factor, k is Boltzmann constant and *T* is absolute temperature.

The sub-threshold slope or the gate voltage swing (SS) describes the turn-on characteristics of the device and is defined as the voltage required increasing the drain current by a factor of 10.
The expression for *SS* is:

$$SS = \frac{\Delta V_{gs}}{\Delta(log I_d)} \qquad (II\text{-}13)$$

In an ideal TFT with no traps or defects in the channel, the subthreshold slope can be as low as 60 mV/decade at room temperature, which is the theoretical limit for a MOSFET device. However, in practical TFTs, the subthreshold slope is often higher due to the presence of traps and defects in the channel, which lead to non-ideal behavior such as hysteresis and leakage

current. The subthreshold slope can be improved by optimizing the device parameters such as the gate oxide thickness, channel doping level, and semiconductor material quality. Thinner gate oxide, higher doping level, and better semiconductor material quality can reduce the density of traps and defects in the channel, leading to lower subthreshold slope and better device performance.

II.5.2.8 Ideality Factor n

The ideality factor (n) in TFTs serves as a metric for assessing the quality of the current-voltage (I-V) characteristics exhibited by the thin-film transistor [86]. It is quantified as the ratio of the measured current to the ideal current corresponding to a given voltage. The ideal current is derived from the equation of the ideal diode, which manifests as a linear relationship with a slope of 1/Vth, where Vth represents the thermal voltage. Significantly, the ideality factor holds significance in TFTs as it profoundly influences the device's performance. A higher ideality factor denotes a superior device, while a lower ideality factor indicates a relatively inferior device. The determination of the ideality factor entails measuring the I-V characteristics of the TFT and fitting the acquired data to the ideal diode equation. Typically, the ideality factor assumes values within the range of n=1 to 2, with 1 being the optimal value.

The ideality factor n is:

$$n = SkT\ ln(10)\ V/decade \qquad (II\text{-}14)$$

A higher ideality factor than 2 indicated defects in the interface that gives rise to increased recombination current. This means that with an ideality factor of 1, the drain current in the sub-threshold region increases one decade if the gate voltage is increased by 60 mV at room temperature 300K.

II.5.2.9 Contact resistance

The source and drain contacts are responsible for carrier injection and extraction and play a critical role in device operation. The active layers of zinc oxide TFTs are generally highly insulating with a high intrinsic carrier concentration.

For others TFTs a heavily doped microcrystalline Si layer is deposited on the active layer in the contact region prior to metallization to improve carrier injection [87]. However, for ZnO-TFTs gaping of the contact region in a conventional sense is not feasible. Therefore,

Schottky source/drain contacts are often made to poly zinc oxide active layer. The formation of an efficient injecting contact requires a suitable match of the work function of the contact metal and the relevant conduction level of semiconductor. With few exceptions, most S-C investigated to date for ZnO-TFTs behave as n-type SC, meaning that the charge transport occurs from a negative towards a positive terminal. Theoretically, these materials should be capable of transporting carries of either type, but structural and chemical defects usually result in the preferred transport of one carrier type over the other. Many of these materials have been classified as Zinc oxide photoconductors with carrier energy gaps, E_g =4.3 eV, E_g Denotes the separation between positive and negative charge carrier conduction levels.

A general rule for forming an ohmic contact to a p-type semiconductor is to use a metal with a work function larger than the conduction level of the SC and Ohmic contacts to n-type SC requires a lower work function than the conduction level of the SC. To select a source and drain contact metals, align the Fermi level E_F, (given by work function of the metal $\emptyset_M$) With the relevant carrier transport level of S-C, Assume a constant vacuum level EVAC [88].

II.5.2.10 Capacitance and frequency response

The significant capacitances between the terminals of ZnO-TFTs are the gate-source and gate-drain capacitances. The drain-source capacitance is much smaller and can usually be ignored.

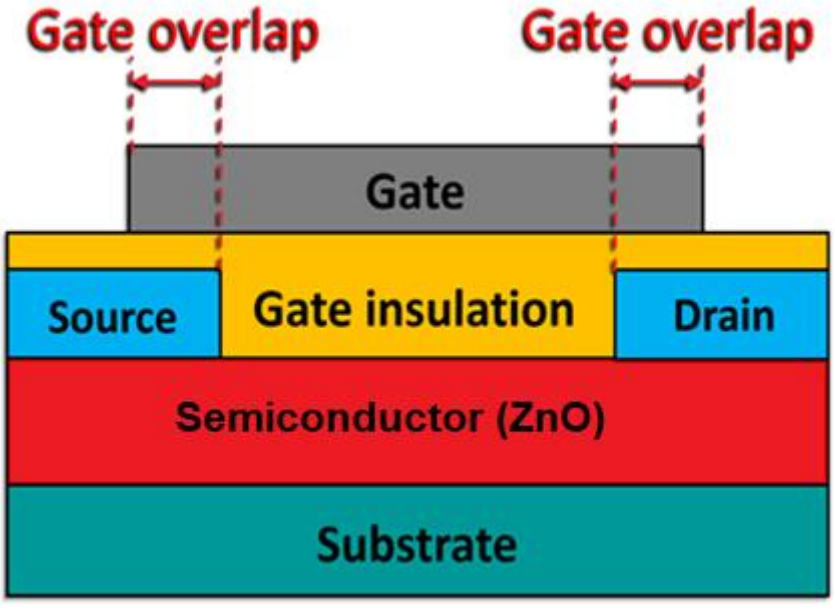


Figure II-12:cross-section ZnO-TFTs show gate overlap.

The gate-source and gate-drain capacitances are each constructed of two capacitances in parallel. One does, to the parasitic overlap capacitance between the gate and the source/drain and the other due to the capacitance between gate and channel. The charge Q is formed on both sides of the isolation gate.

In a TFT, the Q typically refers to the total amount of electric charge stored in the gate dielectric layer between the gate electrode and the channel region of the transistor [89]. This charge is typically expressed in terms of the surface charge density or capacitance per unit area of the dielectric layer. The gate dielectric layer in a TFT serves as a capacitor, with the gate electrode acting as one plate and the channel region acting as the other plate. When a voltage is applied to the gate electrode, a charge is induced on the surface of the dielectric layer, which creates an electric field that modulates the conductivity of the channel region.

The amount of charge stored in the gate dielectric layer determines the strength of the electric field and the degree of modulation of the channel conductivity. Therefore, the charge density in the gate dielectric layer is an important parameter in determining the performance of the TFT, such as the threshold voltage, subthreshold slope, and on/off ratio.

The overlap length can be large and small in TFTs. The reason for the overlap is the fabrication processes used. The overlap capacitance has a limiting effect on the unity gain frequency f_t, at which the transistor current gain falls to unity.
In a simple model this is given by:

$$f_t = \frac{\mu_{FE}(V_{GS}-V_{th})}{2\pi L(L+2L_{overlap})} \qquad (II\text{-}15)$$

When $L_{overlap} \ll$ L as is the case for conventional self-aligned ZnO CMOS processes the maximum operating frequency scales as L^{-2} the well-known ZnO scaling law. Large performance gains then come from reducing the channel length [90].

In high-frequency applications, the frequency response of a TFT is an important parameter that affects the device performance. The frequency response is related to the capacitance and the parasitic resistance and inductance in the device, which can limit the maximum operating frequency.

However, if the amount of overlap is fixed and cannot be reduced, the Si scaling low is

replaced by one in which the maximum operating frequency ultimately scales as L^{-1} . The overlap capacitance could be dramatically reduced if a self-aligned ZnO-TFT process was to be developed.

II.5.2.11 Outline the extraction graphically of TFT output parameters

Thin-film transistors (TFTs) are commonly characterized by various output parameters, including the on-state current (Ion), off-state current (Ioff), threshold voltage (Vth), subthreshold swing, and field-effect mobility at both the linear and saturation regimes. The extraction of output parameters in thin-film transistors (TFTs) plays a crucial role in understanding and optimizing their performance. Several key parameters are commonly extracted to characterize TFT behavior.

The above is summarized in Figure II-13.

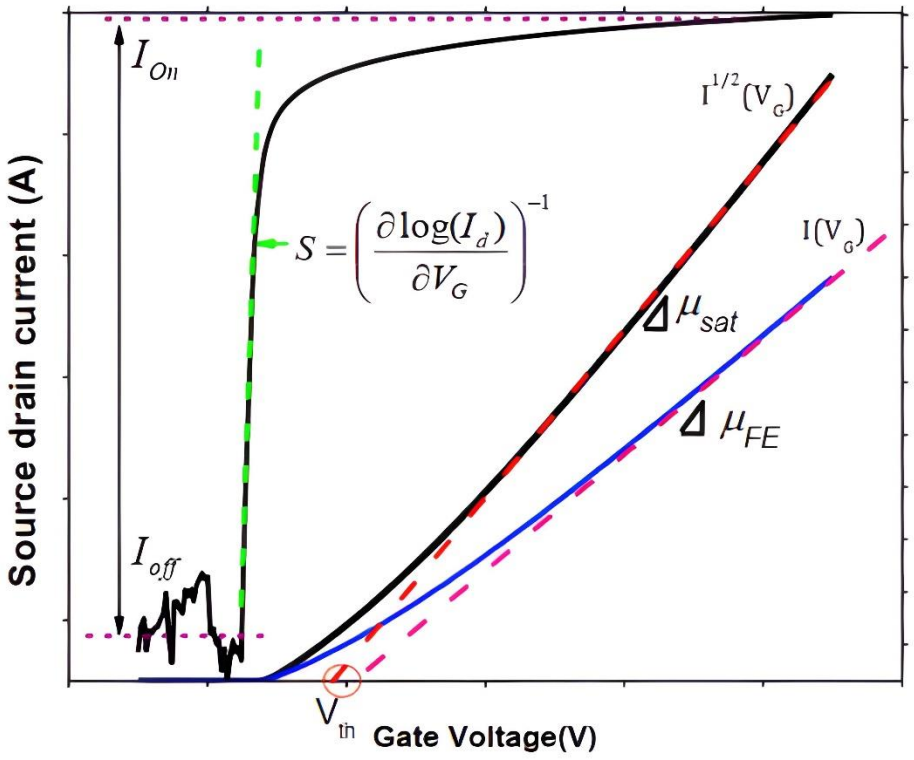


Figure II-13:The extraction methods of TFT output parameters.

To extract these parameters, various measurement techniques and analysis methods are employed. These may involve applying different gate voltages, measuring the drain current, and fitting the data to mathematical models or analytical expressions. Careful calibration and characterization procedures are necessary to ensure accurate parameter extraction and reliable

assessment of TFT performance.

In summary, the extraction of output parameters in TFTs, including the drain current-voltage relationship, Ion and Ioff, Vth, SS, and μ_{FE}, is crucial for understanding and optimizing device performance. Accurate determination of these parameters enables researchers to evaluate the TFT's conduction behavior, switching characteristics, energy efficiency, and charge carrier mobility, contributing to the development of advanced TFT technologies and applications.

II.6 ZnO Thin film transistor fabrication process

The fabrication process of ZnO thin-film transistors (TFTs) involves a series of steps aimed at depositing and patterning the various layers and electrodes to create functional devices. The process begins with the preparation of a suitable substrate, followed by the deposition of a ZnO thin film as the active layer. This is typically accomplished through techniques such as sputtering, chemical vapor deposition (CVD), or sol-gel methods. Once the ZnO thin film is deposited, pattern definition is performed using photolithography techniques, where photoresist materials are applied and selectively exposed to light to define the desired patterns. Subsequently, source and drain electrodes are deposited, typically made of metals such as aluminum (Al) or gold (Au). An insulating layer, often composed of silicon dioxide (SiO_2), is then formed to separate the active layer from the gate electrode, which is also deposited using a suitable material.

II.6.1 Step-by-step explanation of the fabrication process for ZnO TFT

The fabrication process of ZnO thin-film transistors (TFTs) involves several key steps to deposit and pattern the various layers and electrodes [91]. The following is a general overview of the fabrication process for ZnO TFTs:

1. Substrate preparation: Start by preparing a suitable substrate, such as glass or flexible plastic. Clean the substrate thoroughly to remove any contaminants or particles that may affect film quality [92].

2. Deposition of ZnO Thin Film: Deposit the ZnO thin film as the active layer onto the substrate using a deposition technique such as sputtering, chemical vapor deposition (CVD), or sol-gel. Control the deposition parameters to achieve the desired film thickness, uniformity, and crystal structure.

3. Pattern definition: Apply a photoresist material onto the ZnO thin film using spin-coating or other suitable techniques. Expose the photoresist to light through a mask or use a direct writing method to define the desired patterns.

4. Photoresist development: Develop the photoresist by immersing the substrate in a developer solution, which removes the exposed or unexposed regions of the photoresist depending on the type of resist used (positive or negative) [93].

5. Source/Drain electrode deposition: Deposit metal films, such as aluminum (Al) or gold (Au), for the source and drain electrodes using techniques like sputtering, evaporation, or inkjet printing. Define the electrode patterns using a photolithography process similar to the one used for the ZnO thin film.

6. Insulating layer formation: Deposit a thin insulating layer, typically made of silicon dioxide (SiO_2), over the ZnO thin film and the source/drain electrodes [94]. This insulating layer serves as a barrier between the active layer and the gate electrode to prevent direct electrical contact.

7. Gate electrode deposition: Deposit a metal layer, such as aluminum (Al) or indium tin oxide (ITO), as the gate electrode using deposition techniques like sputtering or evaporation. Define the gate electrode pattern using photolithography.

8. Device isolation: Use an isolation technique, such as etching or laser ablation, to electrically isolate individual ZnO TFTs from each other. This step prevents cross-talk and interference between adjacent devices [95].

9. Annealing: Perform an annealing process on the fabricated ZnO TFT structure to improve film crystallinity, remove defects, and enhance electrical properties. Annealing is typically done in a controlled atmosphere, such as a nitrogen or oxygen environment [96].

10. Packaging and testing: Complete the fabrication process by encapsulating the ZnO TFTs to protect them from environmental factors. Perform electrical testing to characterize the device's performance, including threshold voltage, mobility, and on/off ratio.

It's important to note that the specific details of the fabrication process may vary depending on the chosen deposition techniques, device design, and targeted application. Optimizing each step and controlling the process parameters are crucial for achieving high-performance ZnO TFTs.

II.6.2 The key parameters and optimization strategies during the fabrication process ZnO TFT

During the fabrication process of ZnO thin-film transistors (TFTs), several key parameters and optimization strategies play a crucial role in achieving high-performance devices. Here are some important parameters and strategies to consider:

ZnO Thin Film Quality:

- Film thickness: Controlling the thickness of the ZnO thin film is essential for achieving the desired electrical characteristics. It can be optimized based on the specific device requirements.

Crystal Structure:

- The crystallinity of the ZnO thin film affects carrier mobility and overall device performance. Optimization strategies include adjusting the deposition temperature, annealing conditions, and incorporating suitable seed layers or buffer layers [92].

Surface Morphology:

- A smooth and uniform surface is desirable for reducing scattering and improving charge transport. Techniques like surface treatments, buffer layers, and optimized deposition parameters can help achieve an optimized surface morphology [97].

Electrode Materials and Design:

- Source/Drain electrodes: The choice of electrode materials, such as aluminum (Al), gold (Au), or indium tin oxide (ITO), can influence contact resistance and charge injection. Optimizing the electrode material, thickness, and design can enhance the device's electrical properties.

- Gate electrode: The gate electrode material, such as aluminum (Al) or indium tin oxide (ITO),

affects the gate voltage control and capacitance. The gate electrode design, including its dimensions and geometry, can also impact device performance.

Doping:

Doping of the ZnO thin film with suitable impurities can modify its electrical properties, such as carrier concentration and mobility. Doping strategies like intentional incorporation of dopants or post-deposition treatments can be employed to enhance device performance [98].

Annealing:

The annealing process is critical for optimizing the electrical and structural properties of the ZnO thin film. The annealing conditions, including temperature, duration, and atmosphere (e.g., nitrogen, oxygen), need to be carefully controlled to improve crystallinity, remove defects, and enhance carrier mobility [99].

Device dimension and layout:

- The dimensions of the ZnO TFT, such as channel length and width, influence its electrical characteristics. Optimization of these dimensions based on the desired device performance, switching speed, and on/off ratio is important [100].

Process control:

- Optimizing process parameters, such as deposition rates, temperatures, pressures, and durations, is crucial for achieving uniform and reproducible ZnO thin films [101].
- Monitoring and controlling factors like film growth rate, gas flow rates, and substrate cleaning procedures are important for consistent and high-quality TFT fabrication.

Considering and optimizing these key parameters and strategies during the fabrication process of ZnO TFTs, it is possible to enhance device performance, such as carrier mobility, on/off ratio, and reliability. Iterative improvements and thorough characterization are essential for achieving the desired electrical properties and functionality of ZnO TFT-based devices.

II.7 Applications of ZnO thin film transistors

ZnO thin-film transistors (TFTs) have shown great promise for a wide range of

applications due to their unique properties and characteristics. Some notable applications of ZnO TFTs include:

1. Flexible displays: ZnO TFTs offer excellent flexibility, transparency, and high carrier mobility, making them well-suited for flexible display technologies [102]. They can be integrated into flexible substrates, such as plastic or flexible glass, enabling the development of flexible and rollable displays, wearable devices, and curved screens.

2. Sensors: ZnO TFTs can be utilized in various sensing applications [40]. Their high sensitivity, fast response time, and low power consumption make them suitable for gas sensors, chemical sensors, humidity sensors, and biosensors. They can be integrated into smart environmental monitoring systems, healthcare devices, and industrial sensing applications.

3. Integrated circuits (ICs): ZnO TFTs can be employed in the fabrication of integrated circuits [103]. Their high carrier mobility and compatibility with complementary metal-oxide-semiconductor (CMOS) technology make them potential candidates for driving and controlling circuitry in digital logic circuits, memory devices, and signal processing circuits.

4. Transparent electronics: Due to the high transparency of ZnO thin films, ZnO TFTs can be utilized in transparent electronic devices. This includes applications in transparent displays, touchscreens, smart windows, and transparent electrodes for solar cells or optoelectronic devices.

5. Energy harvesting and storage: ZnO TFTs can contribute to energy harvesting and storage devices [104][105]. They can be used in thin-film transistors integrated with photovoltaic cells for energy conversion or in energy storage devices, such as thin-film batteries or supercapacitors.

6. Wearable electronics: ZnO TFTs offer the potential for lightweight, flexible, and wearable electronic devices [106]. They can be incorporated into smart clothing, health monitoring devices, fitness trackers, and biomedical sensors, providing real-time monitoring and data analysis for personalized healthcare and wellness applications.

7. Display backplanes: ZnO TFTs have shown promise as backplane technology for high-resolution displays, such as liquid crystal displays (LCDs) [107] and organic light-emitting diode (OLED) displays [108]. Their high carrier mobility enables faster switching and improved image quality.

The applications of ZnO TFTs are rapidly evolving, and ongoing research and development efforts are exploring new possibilities. As the technology continues to advance, ZnO TFTs are expected to find their way into a wide range of industries, including consumer electronics, healthcare, automotive, aerospace, and more, revolutionizing the way we interact with electronic devices and enabling new functionalities.

II.8 Challenges and future direction

ZnO thin-film transistors (TFTs) hold significant promise for various applications, but they also face several challenges and limitations. Stability, uniformity, and scalability are critical aspects that need to be addressed for the widespread adoption of ZnO TFT technology.

One of the major challenges is stability and reliability. ZnO TFTs can experience degradation over time due to factors such as oxygen and moisture absorption, leading to diminished device performance. Addressing stability issues, including threshold voltage shift and electrical instability, is crucial to ensure long-term reliable operation. Uniformity and yield pose another challenge. Achieving consistent device performance across a large area requires uniform deposition of the ZnO thin film, precise electrode patterning, and control of film quality throughout the substrate. Enhancing uniformity is vital for high yield and manufacturability. Scalability is also a concern for ZnO TFTs. Scaling down the device size while maintaining optimal electrical performance is challenging. Issues such as contact resistance, short-channel effects, and gate leakage become more significant as the dimensions decrease. Developing fabrication techniques and design strategies that address these limitations is essential for scalability.

To overcome these challenges, ongoing research and development efforts are focused on several fronts. Advanced material engineering is being explored, including the development of new ZnO-based materials and alloys with improved stability and mobility. Doping techniques, interface engineering, and novel dielectric materials are also investigated to enhance

performance and stability. Optimizing device architectures is another area of focus. Novel structures like double-gate or multilayer architectures offer better control over the channel region, reducing leakage currents and improving overall device performance. Exploring innovative deposition techniques such as atomic layer deposition (ALD), inkjet printing, and solution processing can enhance film uniformity, thickness control, and scalability. Encapsulation and passivation strategies are crucial for improving stability and reliability. Research is being conducted to develop effective encapsulation materials and techniques that protect ZnO TFTs from environmental factors like moisture and oxygen, ensuring long-term performance. Future directions for ZnO TFTs include advancements in flexible and stretchable electronics. Integrating ZnO TFTs with flexible substrates, exploring new electrode and interconnect materials, and designing stretchable device architectures are important for applications in wearable electronics and conformal displays.

In summary, addressing the challenges of stability, uniformity, and scalability is vital for ZnO TFT technology. Ongoing research and development efforts focus on advanced material engineering, device architecture optimization, novel deposition techniques, encapsulation strategies, and the realization of flexible and stretchable electronics. By overcoming these challenges and exploring new directions, ZnO TFTs can find broader applications across various industries.

Chapter III: SILVACO numerical modeling software

III.1 Introduction

Numerical modeling software plays a pivotal role in the design and optimization of semiconductor devices, offering engineers and researchers a virtual platform to investigate device behavior under various operating conditions. In the realm of thin-film transistors (TFTs), SILVACO stands as a prominent numerical modeling software suite widely utilized for simulating and analyzing device performance [109]. Among the myriad of materials explored for TFT applications, zinc oxide (ZnO) has garnered significant attention.

This introduction focuses on the utilization of SILVACO numerical modeling software for the study of ZnO TFTs. SILVACO provides a comprehensive suite of simulation tools tailored for semiconductor device design, offering capabilities for device modeling, process simulation, and parameter extraction. Through the integration of physical models and algorithms, SILVACO enables researchers and engineers to explore the intricacies of ZnO TFT operation, predict device behavior, and optimize device performance.

III.2 Numerical simulation in TFT

Numerical simulation plays a crucial role in ZnO Thin Film Transistor (TFT) technology by enabling the modeling and analysis of the device's behavior [110]. It serves as a valuable tool for predicting the performance of a TFT device even before it is manufactured. Through the use of computer algorithms and specialized software, the simulation process replicates the physical behavior of the TFT device. This allows researchers to predict its electrical characteristics, including threshold voltage, mobility, and leakage current. Additionally, numerical simulation facilitates the investigation of the impact of various parameters, such as temperature, voltage, and doping concentration, on the device's overall performance. By leveraging these simulations, researchers can optimize the design and performance of ZnO TFTs, contributing to advancements in the field of thin film transistor technology.

The simulation process begins by defining the physical parameters of the device such as its dimensions, material properties, and doping concentration. Then, the device is modeled using a set of equations that describe the physical behavior of the device. The equations are

solved using numerical methods such as finite element analysis or finite difference methods. The numerical solution of the equations provides the electrical characteristics of the device. The simulation results can then be used to optimize the device design and to predict its performance.

To understand the underlying physical mechanisms of an observed phenomenon, a comprehensive approach involving measurement, analysis, and qualitative modeling is necessary. Experimental characterization, although informative, can be a time-consuming process. Analytical modeling, on the other hand, often involves fitting the observed phenomenon to a mathematical model. Alternatively, numerical simulation offers an intriguing alternative as it is cost-effective, efficient, and most importantly, grounded in physical principles. In this study, we employ SILVACO ATLAS [13], a numerical simulation tool, to simulate the current-voltage characteristics of thin-film transistors (TFTs). The chosen approach utilizes the Drift-Diffusion Model (DDM) [14], a widely used model for studying TFT behavior. The DDM is a partial differential equation (PDE)-based model that accounts for the drift and diffusion of electrons and holes within the semiconductor channel of the transistor. The model incorporates the Poisson's equation and steady-state continuity equations to accurately capture the device behavior and investigate the underlying physics, which are given by:

$$div(\varepsilon\nabla\psi) = -\rho = -q(p - n + n_{tail} - p_{tail} + n_{ga} - p_{gd}) \quad \textit{(III-1)}$$

$$0 = \frac{1}{q} div\overrightarrow{J_n} + G_n - R_n \quad \textit{(III-2)}$$

$$0 = -\frac{1}{q} div\overrightarrow{J_p} + G_p - R_p \quad \textit{(III-3)}$$

where ψ is the electrostatic potential, ε is the local permittivity, ρ is the local space charge density, n and p are the free carrier's densities, and n_{tail}, p_{tail}, n_{ga}, p_{gd} (the DOS constituents) are given by:

$$n_{tail} = \int_{E_v}^{E_c} g_{ct}^{A}(E) f_{ct}^{n}(E)\, dE \quad \textit{(III-4)}$$

$$p_{tail} = \int_{E_v}^{E_c} g_{vt}^{D}(E) f_{vt}^{p}(E)\, dE \quad \textit{(III-5)}$$

$$n_{ga} = \int_{E_v}^{E_c} g_{G}^{A}(E) f_{AG}^{n}(E)\, dE \quad \textit{(III-6)}$$

$$p_{gd} = \int_{E_v}^{E_c} g_{G}^{D}(E) f_{DG}^{p}(E)\, dE \quad \textit{(III-7)}$$

where $f_{ct}^{n}(E)$, $f_{AG}^{n}(E)$ are the ionization probabilities of the acceptor tail and Gaussian

states, respectively, and $f_{vt}^{p}(E)$, $f_{DG}^{p}(E)$ are the ionization of the donor states (tail and Gaussian). At the steady state, these ionization probabilities are given by the Shockley-Read-Hall (SRH) model:

$$f_{ct}^{n}(E) = \frac{v_{th}^{n}\sigma_{nc}n + v_{th}^{p}\sigma_{pc}n_i e^{\frac{E_i - E}{k_B T}}}{v_{th}^{n}\sigma_{nc}\left(n + n_i e^{\frac{E - E_i}{k_B T}}\right) + v_{th}^{p}\sigma_{pc}\left(p + n_i e^{\frac{E_i - E}{k_B T}}\right)} \quad (III\text{-}8)$$

$$f_{AG}^{n}(E) = \frac{v_{th}^{n}\sigma_{ng}^{a}n + v_{th}^{p}\sigma_{pg}^{a}n_i e^{\frac{E_i - E}{k_B T}}}{v_{th}^{n}\sigma_{ng}^{a}\left(n + n_i e^{\frac{E - E_i}{k_B T}}\right) + v_{th}^{p}\sigma_{pg}^{a}\left(p + n_i e^{\frac{E_i - E}{k_B T}}\right)} \quad (III\text{-}9)$$

$$f_{vt}^{p}(E) = \frac{v_{th}^{p}\sigma_{pv}p + v_{th}^{n}\sigma_{nv}n_i e^{\frac{E - E_i}{k_B T}}}{v_{th}^{n}\sigma_{nc}\left(n + n_i e^{\frac{E - E_i}{k_B T}}\right) + v_{th}^{p}\sigma_{pc}\left(p + n_i e^{\frac{E_i - E}{k_B T}}\right)} \quad (III\text{-}10)$$

$$f_{DG}^{p}(E) = \frac{v_{th}^{p}\sigma_{pg}^{d}p + v_{th}^{n}\sigma_{ng}^{d}n_i e^{\frac{E - E_i}{k_B T}}}{v_{th}^{n}\sigma_{ng}^{d}\left(n + n_i e^{\frac{E - E_i}{k_B T}}\right) + v_{th}^{p}\sigma_{pg}^{d}\left(p + n_i e^{\frac{E_i - E}{k_B T}}\right)} \quad (III\text{-}11)$$

where v_{th}^{n} is the electron thermal velocity and v_{th}^{p} is the hole thermal velocity, n_i is the intrinsic carrier concentration, σ_{nc} and σ_{ng}^{a} are the electron capture cross-section for the acceptor tail and Gaussian states respectively, σ_{pc} and σ_{pg}^{a} are the hole capture cross-sections for the acceptor tail and Gaussian states respectively and σ_{nv}, σ_{ng}^{d}, σ_{pv}, and σ_{pg}^{d} are the equivalents for donors states.

$\overrightarrow{J_n}$ and $\overrightarrow{J_p}$ are the electrons and holes current densities are given by:

$$\overrightarrow{J_n} = qn\mu_n\vec{E} \quad (III\text{-}12)$$

$$\overrightarrow{J_p} = qp\mu_p\vec{E} \quad (III\text{-}13)$$

Then the total drift current density is:

$$\vec{J} = q(n\mu_n + p\mu_p)\vec{E} \quad (III\text{-}14)$$

Where μn and μp are electron and hole mobilities, respectively. $\vec{E}$ is electric field.

G_n and G_p are the generation rates for electrons and holes which are neglected in this

study, R_n and R_p are the total recombination rates for electrons and holes in Gaussian and tail states, and q is the electron charge. R_n and R_p are assumed to be the same and given by [15]:

$$R_n = R_p = \int_{E_V}^{E_C}(np - n_i^2)\left\{\left[\frac{v_{th}^n v_{th}^p \sigma_{pc}\,\sigma_{nc} g_{ct}^A(E)}{v_{th}^n \sigma_{nc}\left(n+n_i e^{\frac{E-E_i}{k_B T}}\right)+v_{th}^p \sigma_{pc}\left(p+n_i e^{\frac{E_i-E}{k_B T}}\right)}\right]+\left[\frac{v_{th}^n v_{th}^p \sigma_{pv}\,\sigma_{nv} g_{vt}^D(E)}{v_{th}^n \sigma_{nv}\left(n+n_i e^{\frac{E-E_i}{k_B T}}\right)+v_{th}^p \sigma_{pv}\left(p+n_i e^{\frac{E_i-E}{k_B T}}\right)}\right]+\left[\frac{v_{th}^n v_{th}^p \sigma_{pg}^a \sigma_{ng}^a g_G^A(E)}{v_{th}^n \sigma_{ng}^a\left(n+n_i e^{\frac{E-E_i}{k_B T}}\right)+v_{th}^p \sigma_{pg}^a\left(p+n_i e^{\frac{E_i-E}{k_B T}}\right)}\right]+\left[\frac{v_{th}^n v_{th}^p \sigma_{pg}^d \sigma_{ng}^d g_G^D(E)}{v_{th}^n \sigma_{ng}^d\left(n+n_i e^{\frac{E-E_i}{k_B T}}\right)+v_{th}^p \sigma_{pg}^d\left(p+n_i e^{\frac{E_i-E}{k_B T}}\right)}\right]\right\} dE \quad \textit{(III-15)}$$

By solving the above equations simultaneously, the drift-diffusion model can predict the behavior of TFTs under different operating conditions, such as gate voltage, bias voltage, temperature, and doping concentration. It is a powerful tool for designing and optimizing TFTs for various applications, including displays, sensors, and integrated circuits.

In the linear region ($V_{DS}<V_{GS}$) the drain current can be written as:

$$I_{DS} = C_{ox}\mu_{FE}\frac{W}{L}(V_{GS} - V_{th})V_{DS} \quad \textit{(III-16)}$$

Where C_{ox} is the capacitance per (unit area) of the gate insulator, μ_{FE} is the field-effect mobility, W and L are the channel width and the length, respectively, and V_{th} is the threshold voltage.

The activation energy of electrons, E_a, as a function of temperature, can be calculated from the Arrhenius equation [16]:

$$I = I_{298}e^{\frac{-E_a}{KT}} \quad \textit{(III-17)}$$

Where I_{298} is the room temperature current. E_a is the activation energy of electrons and k is Boltzmann constant , T is absolute temperature.

In a thin-film transistor (TFT), the transport behavior is governed by three fundamental

equations: Poisson's equation and the continuity equations for electron and hole transport. These equations need to be satisfied at every point within the device, and solving them involves determining the values of variables such as electron concentration (n(x)), hole concentration (p(x)), and electric potential (ψ(x)) at each point x, which fully characterizes the system. However, these governing equations are nonlinear and coupled, making them unsolvable analytically. Therefore, numerical methods such as Newton's method are employed to numerically solve the resulting equations. Just like any mathematical analysis, appropriate boundary conditions must be imposed on all equations. These conditions ensure that the solutions of the equations satisfy the specified requirements at the boundaries of the device.

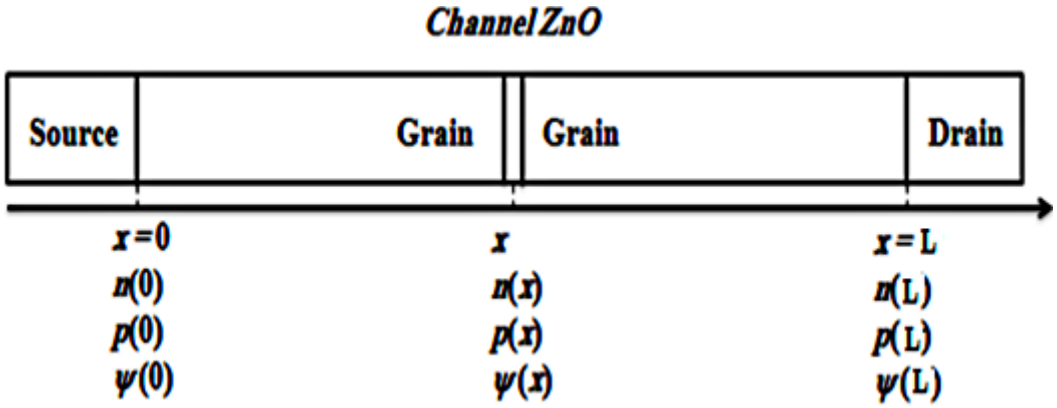


Figure III-1:Boundary conditions for the nc-ZnO TFT simulated in this work.

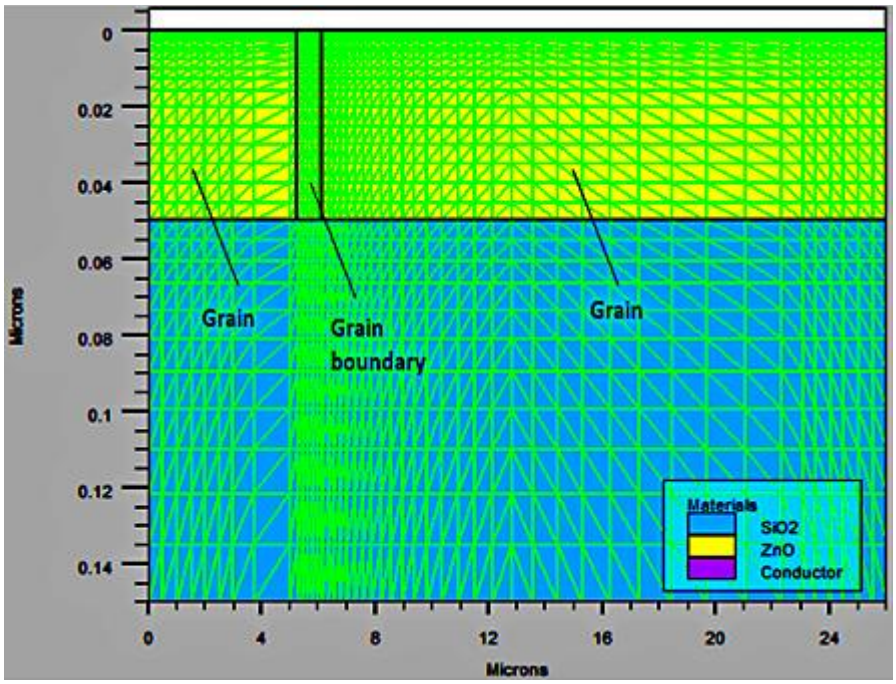


Figure III-2:2D mesh grain and grain boundary of ZnO TFT.

The initial conditions are arbitrary conditions, which must check boundary conditions at the limits. For simplicity, we can consider linear distributions for the potential ψ and the densities of the electrons and holes to liberate n and p.

$$\psi(x) = A.x + B \qquad \textit{(III-18)}$$

$$n(x) = n(0)exp\left(\frac{q\psi(x)}{k_\beta T}\right) \qquad \textit{(III-19)}$$

$$p(x) = p(0)exp\left(-\frac{q\psi(x)}{k_\beta T}\right) \qquad \textit{(III-20)}$$

Where A, B are constants calculated from initial conditions.

To solve these equations (1,2,3), numerical methods must be used to find possible results. In this case, we use two methods iteration: the Gummel's and Newton's method[14]-[15].

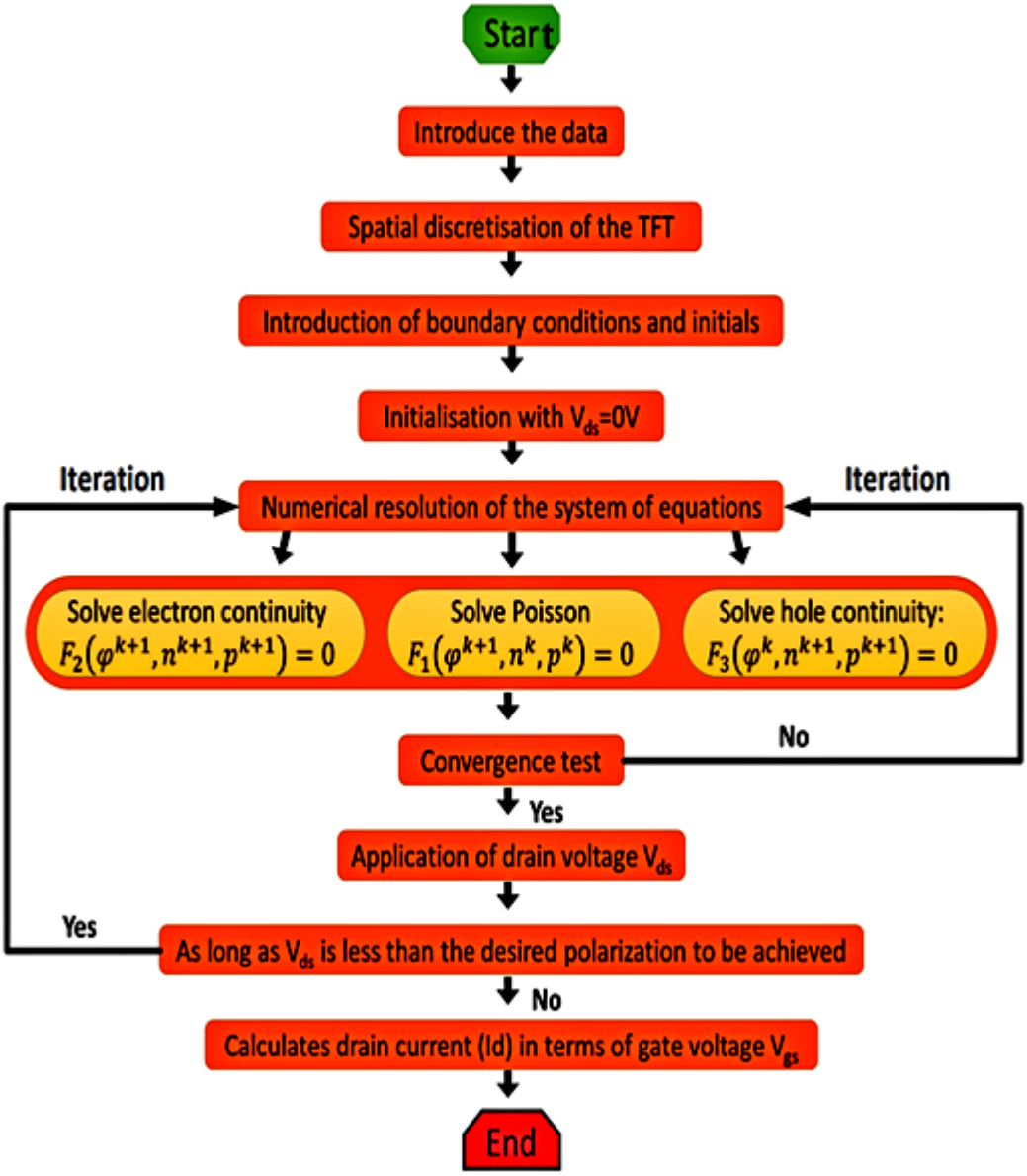


Figure III-3:Flowchart of the digital resolution procedure in Atlas of the ZnO TFT by way of repetition.

k is indicating the number of iterations.

The Gummel's method solves the coupled set of semiconductor equations[117]; it solves the system of drift-diffusion equations via a decoupled procedure. First, the solution of the poison's equation is resolved separately at equilibrium (zero voltage) to calculate the surface potential. The solution of Poisson's equation is necessary, since the equilibrium Fermi level is constant and coincides with both quasi-Fermi levels [118].

Newton's method is a numerical algorithm used to solve nonlinear equations, such as the equations used in the simulation of thin-film transistors (TFTs) [10]. In the context of TFT

simulations, Newton's method is commonly used to solve the Poisson's equation and the continuity equations for electrons and holes. The basic idea behind Newton's method is to iteratively refine an initial guess of the solution until it converges to the actual solution. The iteration process continues until the residual is small enough, indicating that the solution has converged to the actual solution. Once the potential is known, the electron and hole concentrations can be obtained by solving the continuity equations using the updated potential.

In general, the Gummel's method is useful when the system of equations is weak but has only a linear affinity. The Newton's method is useful when the equation system is strongly coupled and has a quadratic affinity. However, the Newton's method may spend additional time solving quantities, which are essentially constant or double. Gummel can provide best first guesses for problems. It may be helpful to start a solution with some duplicates of Gummel to create an optimal guess. Then, go to Newton's to complete the solution. It will cause the solver to start with Gummel iterations. Then, switch to Newton's if convergence is not achieved. This is a robust but a more time consuming way of obtaining solutions for any device[111]. The mixed method is used in our research.

In conclusion, numerical simulation in TFT technology is an important tool for the development of new TFT devices. It is used to study the effects of various parameters on the device's performance and to optimize the device design. It is also used to verify the design of the device before it is actually manufactured. The simulation process can also be used to predict the performance of a device under different operating conditions.

III.3 Simulation by SILVACO TCAD

Silvaco TCAD is a software package that is widely used for simulating the performance of thin-film transistors (TFTs). The software allows users to create 2D or 3D models of the TFT structure and simulate the electrical and optical behavior of the device under different operating conditions. Some of the key simulations that can be performed using Silvaco TCAD for TFTs include:

1. Device structure simulation: The software can be used to create a detailed 2D or 3D model of the TFT structure, including the channel, source, and drain regions, gate dielectric, and metal contacts.

2. Electrical simulation: Silvaco TCAD can simulate the electrical behavior of the

TFT, including the current-voltage (I-V) characteristics, threshold voltage, subthreshold swing, and mobility.

3. Optical simulation: The software can also simulate the optical properties of the TFT, including the reflectance, transmittance, and absorption spectra.

4. Process simulation: Silvaco TCAD can simulate the entire fabrication process of the TFT, including the deposition of the various layers, lithography, and etching steps.

SILVCO TCAD includes many modules for the simulation of semiconductor devices such as ATHENA and ATLAS. ATHENA is used to simulate the fabrication process while ATLAS is for the electrical device performance. ATHENA and ATLAS work under platform called DECKBUILD. DECKBUILD is an interactive, graphic runtime environment for developing process and device simulation input decks. Figure III-4 shows the DECKBUILD window. It is considered as the principal window of SILVACO where all simulators can be controlled.

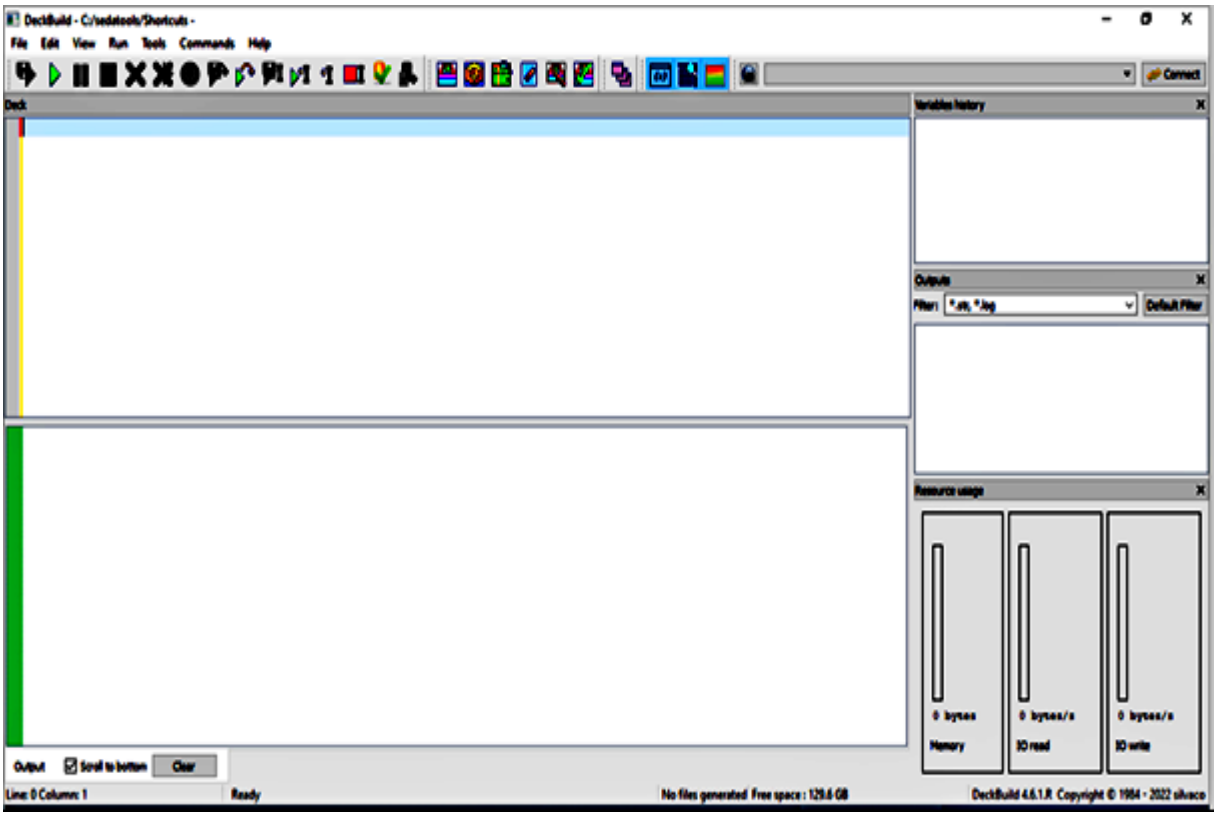


Figure III-4: DECKBUILD window SILVACO 2018.

The software is also capable of performing advanced analysis, such as Monte Carlo simulations, which can be used to analyze the statistical behavior of semiconductor devices. It can also be used to analyze the performance of integrated circuits, as well as to optimize the design of semiconductor devices. Overall, SILVACO ATLAS is a powerful and versatile simulation tool for semiconductor device modeling and analysis. It is capable of simulating a wide range of device types, and can be used to analyze the performance of integrated circuits and optimize the design of semiconductor devices.

The obtained results plotted and analyzed by another tool named TONYPLOT. TONYPLOT is a visualization tool which plots the results obtained from simulation. It provides scientific visualization capabilities including xy plots with linear and logarithmic axes, polar plots, surface and contour plots. Figure III-5 shows process SILVACO simulation steps by and the module used for each step.

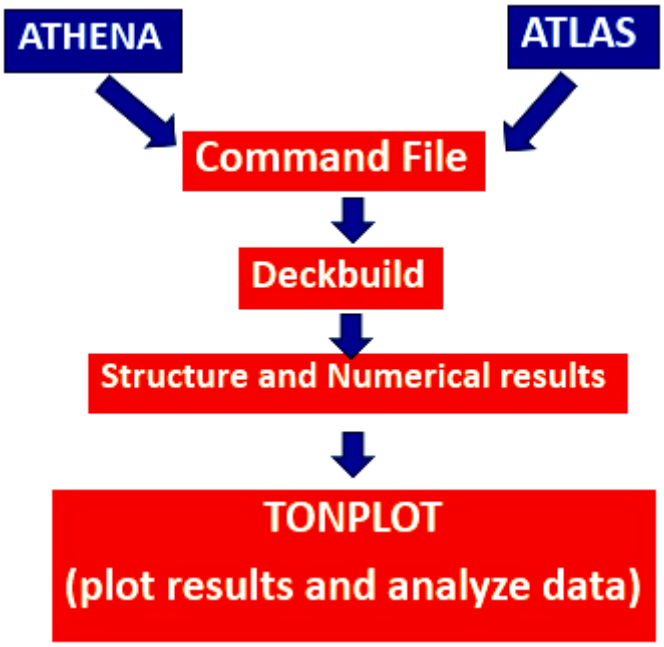


Figure III-5: Process of simulation by SILVACO.

The process of simulating a ZnO TFT using SILVACO typically involves the following steps:

1. Designing the device structure: The first step in simulating a ZnO TFT is to define the device structure, including the dimensions of the channel, source, drain, and gate electrodes, as well as the thickness and material properties of the various layers in the device stack. This information is typically input into the software using a graphical user interface or text-based input file.

2. Defining the material properties: The next step is to specify the material properties of the various layers in the device stack, including the ZnO semiconductor layer, the gate dielectric layer, and any other layers such as the source/drain contacts or passivation layers. This information is typically obtained from experimental measurements or theoretical calculations, and is input into the software using a database or material properties file.

3. Setting the simulation parameters: Once the device structure and material properties have been defined, the simulation parameters must be set, including the bias conditions (i.e., the voltages applied to the source, drain, and gate electrodes), the temperature, and any other relevant parameters such as the

doping concentration or carrier mobility.

4. Running the simulation: With the device structure, material properties, and simulation parameters defined, the simulation can be run using the SILVACO software. This typically involves solving a set of nonlinear partial differential equations that describe the behavior of the semiconductor material and the electric fields within the device, and calculating the resulting current flow and other electrical characteristics of the TFT.

5. Analyzing the results: Once the simulation has been completed, the results can be analyzed using various tools and techniques, such as plotting current-voltage characteristics, analyzing the field distribution within the device, or comparing the simulated results to experimental measurements. This analysis can help to refine the device design and optimize the performance of the ZnO TFT.

III.3.1 Commands File

Command file or Atlas input is a file which contains commands and statements for simulation. This file can be written in the DECKBUILD environment or another program but must run by DECKBUILD. The order in which statements occur in an ATLAS input file is important. There are five groups of statements that must occur in the correct order (see Table III-1). Otherwise, an error message will appear which may cause incorrect operation or termination of the program.

Table III-1:The order of Atlas commands.

Groups	Statements
Structure specification	MESH REGION ELECTRODE DOPING
Material and models specification	CONTACT MATERIAL INTERFACE MODELS
Numerical method selection	METHOD

Solution specification	SOLVE SAVE
Results analysis	TONYPLOT

III.3.1.1 Structure specification

Each Atlas run inside DECKBUILD should start with the line: go atlas

<n>.MESH specifies the location of grid lines along the <n>-axis in a rectangular mesh for 2D or 3D simulation.

Syntax X.MESH LOCATION=<l> (NODE=<n> [RATIO=<r>])| SPACING=<v>

WIDTH Specifies the extent of a mesh section in the X direction.

X.MIN/Y.MIN Specify the location of the beginning of a given mesh section (should only be specified for the first section).

X.MAX/Y.MAX Specify the location of the end of a given mesh section (should not be specified if DEPTH/WIDTH is specified).

Region Parameters Device coordinates may be used to add regions to both rectangular and irregular meshes. In either case, boundaries must be specified with the X.MAX, X.MIN, Y.MAX, Y.MIN, Z.MAX, and Z.MIN parameters.

Once the mesh is specified, every part of it must be assigned a material type. This is done with REGION statements:

REGION number=<integer> <material_type> <position parameters>

Region numbers must start at 1 and are increased for each subsequent region statement. A large number of materials is available. The position parameters are specified in microns using the X.MIN, X.MAX, Y.MIN, and Y.MAX parameters.

MATERIAL Specifies what material from atlas know materials the statement should apply. If a material is specified, then all regions defined as being composed of that material will be affected.To define mesh and structure of TFT poly-ZnO with SiO_2. And n-poly Si as gate, Al was used as Aluminum source and drain. Use the following code source.

```
go atlas
mesh width=180 outf=tft.str master.out
x.m l=0 s=0.25
x.m l=40 s=0.25
y.m l=0 s=0.0005
y.m l=0.025 s=0.0005
y.m l=0.12 s=0.005
# The device is composed of a 25 nm layer of zno
# 100 nm oxide on a n++ substrate that acts as the gate.
region num=1 material=zno y.min=0 y.max=0.025
```

```
region num=2 material=sio2 y.min=0.025 y.max=0.12
elec num=1 name=gate bottom
elec num=2 name=source y.max=0.0 x.min=0.0 x.max=5.0
elec num=3 name=drain y.max=0.0 x.min=35.0 x.max=40
```

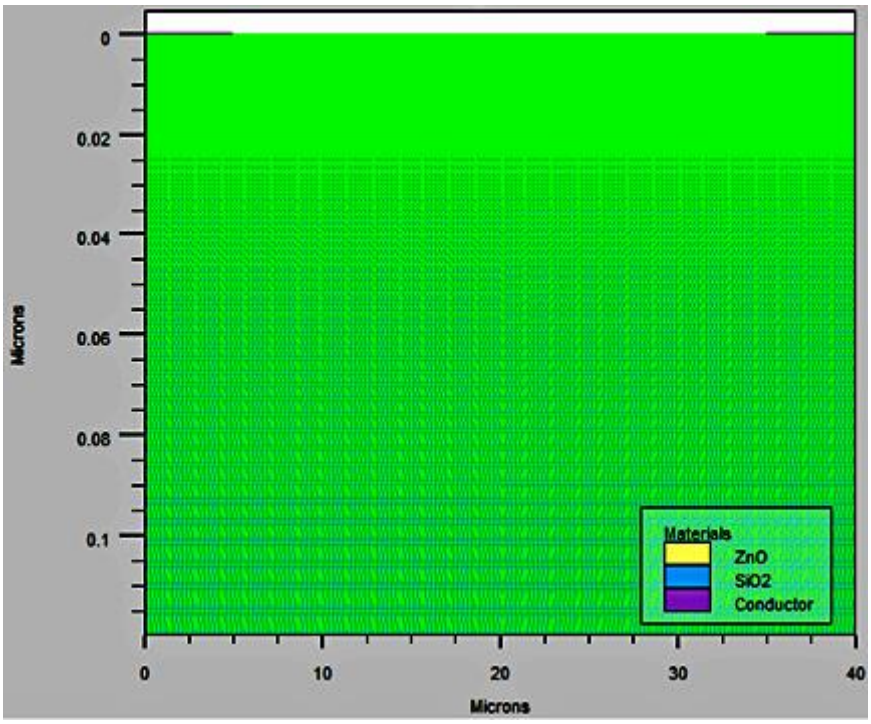


Figure III-6 and Figure III-7 show mesh and structure of 2D poly-ZnO TFT generated by using the above code source.

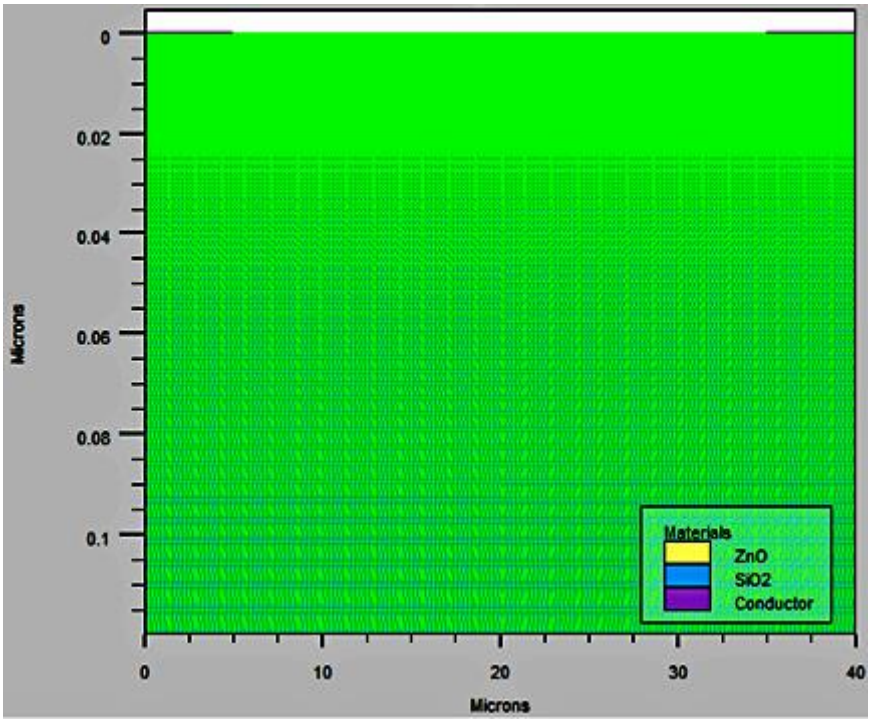


Figure III-6:2D mesh poly-ZnO TFT.

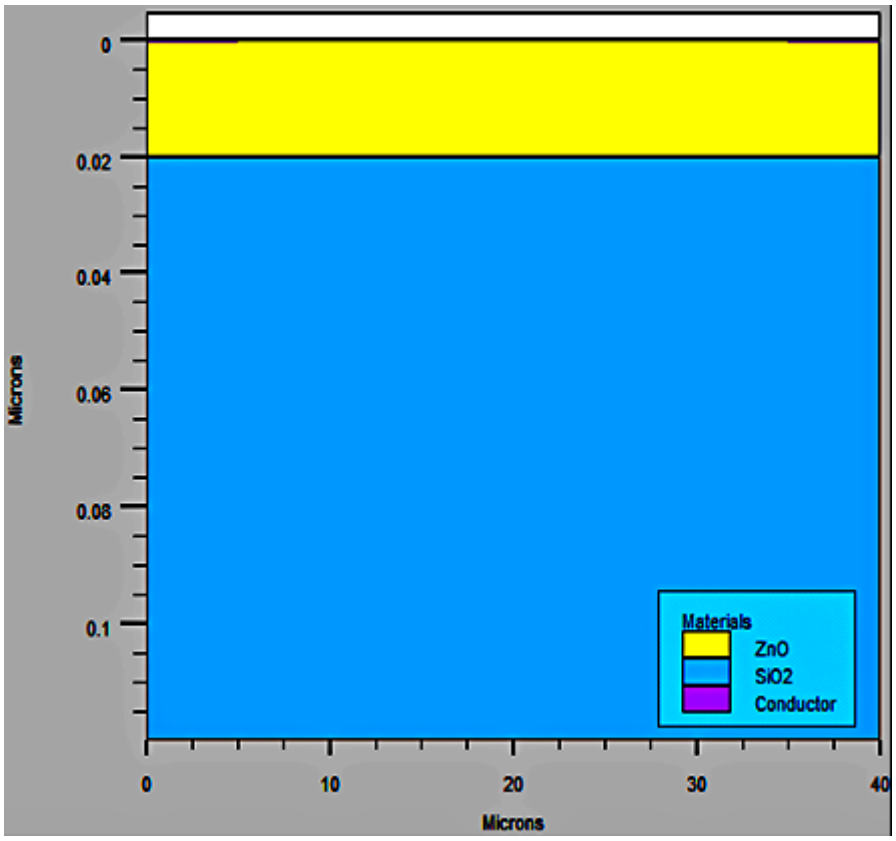


Figure III-7: 2D structure of poly-ZnO TFT.

III.3.2 Material and model's specification

In this part physical parameters of each material must be specified. Some materials are already known by SILVACO ATLAS but some other material need definition or adjusting their parameters.

The CONTACT statement is used to specify the metal work function of one or more electrodes. The NAME parameter is used to identify which electrode will have it is properties modified. The WORKFUNCTION parameter sets the work function of the electrode. Example:

CONTACT NAME=gate WORKFUNCTION=4.08

The statement of the work function for a n-type polysilicon gate contact is: CONTACT NAME=gate N.POLYSILICON

The following statement "MATERIAL MATERIAL=" is used to adjust physical parameters of material.

The DEFECTS statement is used to describe the density of defect states in the band gap. One can specify up to four distributions, two for donor-like states and two for acceptor-like states.

Each type of state may contain one exponential (tail) distribution and one Gaussian distribution. DEFECTS activate the band gap defect model and sets the parameter values. This model can be used when thin-film transistor simulations are performed using the TFT product. The Syntax DEFECTS [<parameters>]

Egd: Specifies the energy that corresponds to the Gaussian distribution peak for donor-like states. This energy is measured from the valence band edge.

Ngd: specifies the total density of donor-like states in a Gaussian distribution.

Nta: Specifies the density of acceptor-like states in the tail distribution at the conduction band edge.

Ntd: Specifies the density of donor-like states in the tail distribution at the valence band edge.

Wgd: Specifies the characteristic decay energy for a Gaussian distribution of donor-like states.

Wta: Specifies the characteristic decay energy for the tail distribution of acceptor-like states.

Wtd: Specifies the characteristic decay energy for the tail distribution of donor-like states.

SIGGAE: Specifies the capture cross-section for electrons in a Gaussian distribution of acceptor-like states.

SIGGAH: Specifies the capture cross-section for holes in a Gaussian distribution of acceptor-like states.

SIGGDE: Specifies the capture cross-section for electrons in a Gaussian distribution of donor-like states.

SIGGDH: Specifies the capture cross-section for holes in a Gaussian distribution of donor-like states.

SIGTAE: specifies the capture cross-section for electrons in a tail distribution of acceptor-like states.

SIGTAH: Specifies the capture cross-section for holes in a tail distribution of acceptor-like states.

SIGTDE: Specifies the capture cross-section for electrons in a tail distribution of donor-like states.

SIGTDH: Specifies the capture cross-section for holes in a tail distribution of donor-like states.

The poly-ZnO TFT regions, materials, electrodes and work function definition are as follows:

```
# We define the gate as N.POLY
contact num=1 n.poly
# We also define a workfunction for the source and drain that
# is very close to the conduction edge
contact num=2 ALUMINUM workf=4.08
contact num=3 ALUMINUM workf=4.08
MATERIAL MATERIAL=zno eg300=3.4 mun=40 mup=1.5
```

```
models fermi
# Key to the characterization of amorphous materials is the
# definition of the states within the band gap.
defects region=1 nta=3.6e21 ntd=4.0e19 wta=0.12 wtd=0.1 \
        nga=1.0e19  ngd=1.0e19 egd=0.14 wgd=0.15 \
        sigtae=4e-15 sigtah=4e-15 sigtde=4e-15 sigtdh=4e-15 \
        siggae=4e-15 siggah=4e-15 siggde=4e-15 siggdh=4e-15 \
        dfile=tftdon.dat afile=tftex10acc.dat numa=128 numd=128
```

III.3.2.1 Numerical method selection

Several different numerical methods can be used for calculating the solutions of semiconductor device problems. Numerical methods are given in the METHOD statement of the input file. Some guidelines for these methods will be given here. Different combinations of models will require ATLAS to solve up to six equations. For each of the model types, there are basically three types of solution techniques: (a) decoupled (GUMMEL), (b) fully coupled (NEWTON) and (c) BLOCK. If any one of the methods is not chosen, ALTAS will use newton method to solve the equations. Specification of the solution method is carried out as follows:

```
METHOD GUMMEL BLOCK NEWTON
```

III.3.2.2 Solution specification

An initial state without any voltage applied is assumed by usine the “solve init” command; Secondly, for an applied voltage between source and drain, the equation is solved using the” solve vdrain” command.

the command outf and save used to save solution in file or structure respectively.

```
# From here we simply extract the Id-Vg characteristic
solve init
solve prev
solve vdrain=1
solve vdrain=5
save outf=tft.str
log outf=tfa.log
solve vgate=0 vstep=-0.2 vfinal=-04.0 name=gate
log off
load inf=tft.str master
solve prev
log outf=tfb.log
solve vstep=1 vfinal=40.0 name=gate
log off
```

III.3.2.3 Results analysis

The statement tonyplot is used to plot Id-Vg characteristic.

```
#Plotting Id-Vg characteristic
tonyplot -overlay tfta.log tftexb.log
```

Figure III-8 shows the resulting graph by tonyplot command.

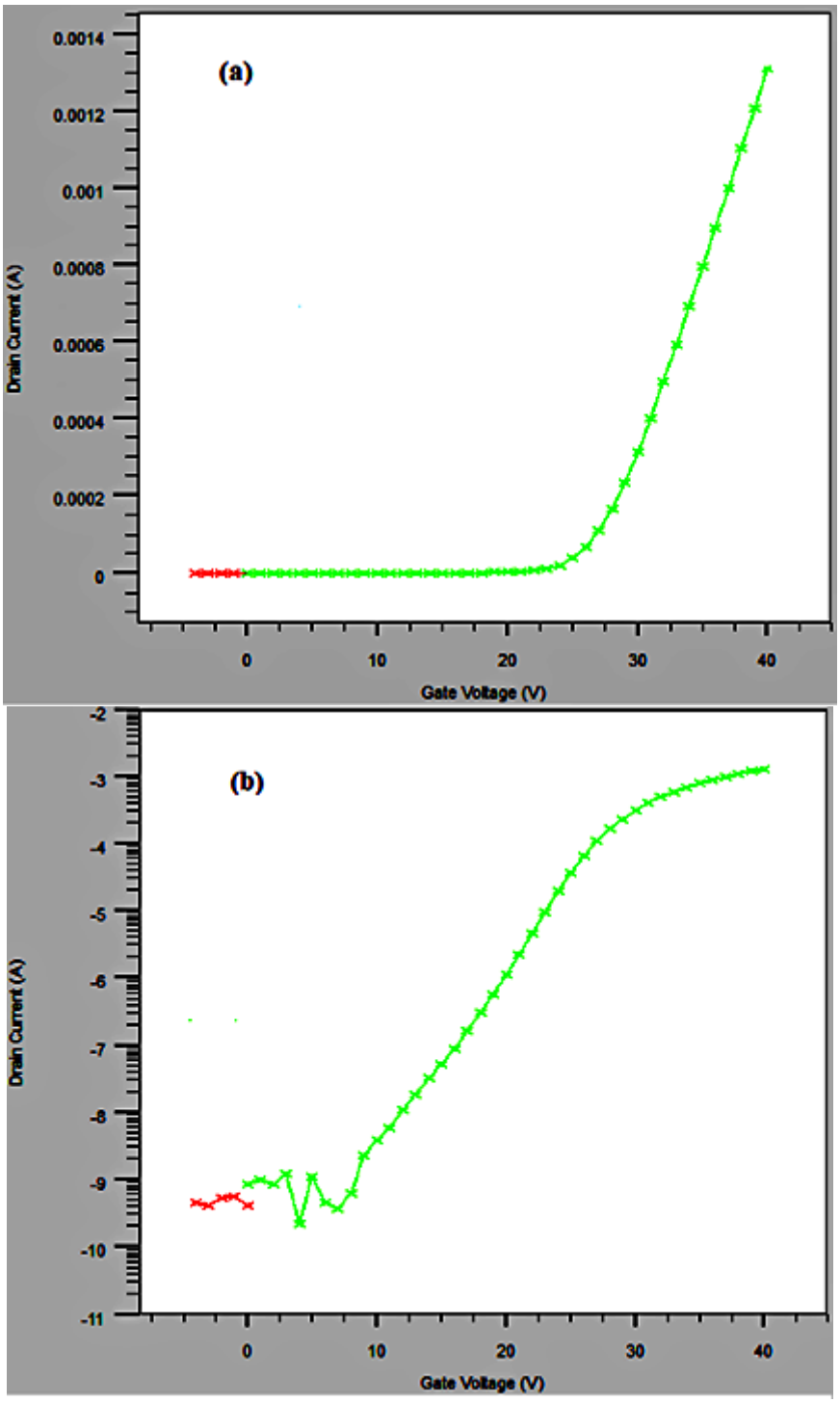


Figure III-8: Id-Vg characteristics (a linear and b logarithm).

In summary, the process of simulating a ZnO TFT using SILVACO software involves

designing the device structure, defining the material properties of the various layers, setting the simulation parameters, running the simulation, and analyzing the results. SILVACO is used to solve the nonlinear partial differential equations that describe the behavior of the semiconductor material and the electric fields within the device, and to calculate the resulting current flow and other electrical characteristics of the TFT. The simulation results can be analyzed to refine the device design and optimize the performance of the ZnO TFT.

Chapter IV: Results and discussion

IV.1 Introduction

In this chapter, we will discuss four distinct studies that contribute to the understanding and improvement of TFT technology.

1. Effect of temperature on pc-ZnO TFT.
2. Effect of defect creation by illumination on pc-ZnO TFT at low temperature.
3. Effects of nano-grain size and boundary on nc-ZnO TFTs related to deposition. temperature.
4. Fabrication and characterization of ZnO thin film transistors by PVD deposition method.

IV.2 Effect temperature at pc-ZnO TFT

IV.2.1 Modeling and simulation of ZnO TFT

A three dimensional cross section of the ZnO TFT structure used in this work is shown in Figure IV-1 and is similar to experimental work [11] for comparison. The conducting n-type channel is made of a 25 nm thick ZnO, heavily doped n-type poly-silicon is used as the substrate as well as the gate, silicon oxide (SiO_2) isolates the gate from the channel is a 280 nm thick, the drain and source ohmic contacts are 5 µm long aluminium (Al) and 35 µm from each other. The whole structure width is 2 mm.

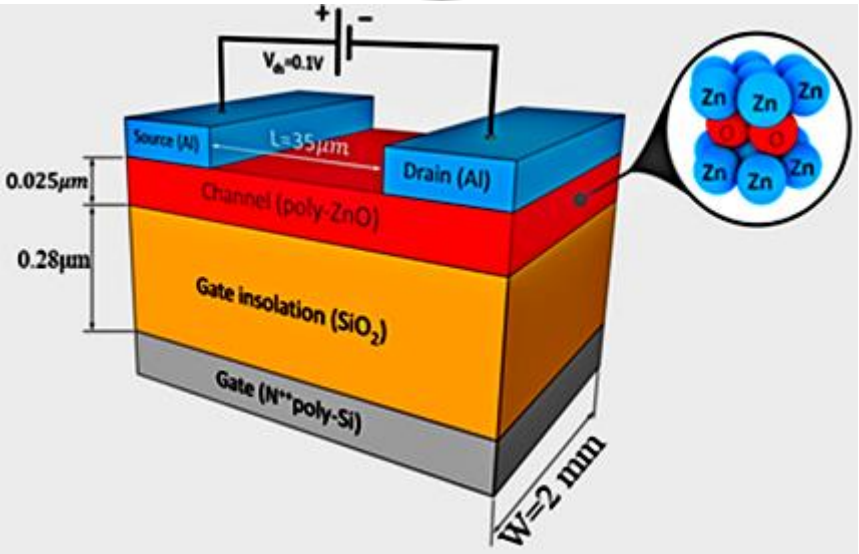


Figure IV-1:A three-dimensional view of the pc-ZnO TFT simulated in this work.

The channel is made of ZnO which is a poly-crystalline n-type semiconductor. Its electronic properties (density of states in the gap or DOS) are usually similar to those of amorphous hydrogenated silicon (a-Si:H) and amorphous indium gallium zinc oxide (a-IGZO) [9,12]. The DOS is composed of acceptor like states (near the conduction band) given by the sum of tail states and deep states $\left(g_{ct}^{A}(E)+g_{G}^{A}(E)\right)$, and donor-like states (near the valence band) given by the sum of tail states and deep states. $\left(g_{vt}^{D}(E)+g_{G}^{D}(E)\right)$. The total DOS distribution g(E) is then given by:

$$g(E) = g_{ct}^{A}(E)+g_{G}^{A}(E) + g_{vt}^{D}(E) + g_{G}^{D}(E)$$
$$= g_{ta}exp\left(\frac{E-E_C}{E_a}\right) + g_{td}exp\left(\frac{E_V-E}{E_d}\right) + g_{gd}exp\left(-\frac{(E-E_D)^2}{\sigma_D^2}\right) + g_{ga}exp\left(-\frac{(E_A-E)^2}{\sigma_A^2}\right) \qquad (IV\text{-}1)$$

where $g_{ta}(cm^{-3}eV^{-1})$ is the effective density at E_C, and E_a is the characteristic slope energy of the conduction band-tail states, $g_{td}(cm^{-3}eV^{-1})$ is the effective density at E_V, and E_d is the characteristic slope energy of the valence band-tail states, $g_{gd}\left(g_{ga}\right)$, are the total density $(cm^{-3}eV^{-1})$, $\sigma_D(\sigma_A)$ the standard deviation and $E_D(E_A)$ the peak energy of the Gaussian distribution.

The electrical characteristics are calculated following the specified physical structure and bias conditions. Of interest to the present work, the current-voltage characteristics are calculated for different temperatures. The DOS parameters used for this model extracted in accordance with the experimental work are shown in Table IV 1. The other values were set to

the default ATLAS values for pc-ZnO.

Table IV-1:The parameters of the DOS model in pc-ZnO used in this work.

Parameter	**Value**
Electron affinity	4.29 eV
Dielectric constant	8.12
Electron mobility	40 $cm^2/V.s$
Hole mobility	1.5 $cm^2/V.s$
Effective conduction band states	4.3 10^{18} cm^{-3}
Effective valence band states	4.3 10^{18} cm^{-3}
Energy gap at 300K	3.4 eV
Density of acceptor-like tail states	3.6 10^{21} $cm^{-3}.eV^{-1}$
Density of donor-like tail states	4 10^{19} $cm^{-3}.eV^{-1}$
Capture cross section of electron and hole states	4.0 10^{-15} cm^2
Characteristic decay energy acceptor-like tail states	0.12 eV
Characteristic decay energy donor-like tail states	0.1 eV

Comparison between experimental[122] and simulated transfer characteristics of pc-ZnO thin-film transistors are shown in Figure IV-2 at 298 K. This shows a good agreement and this is perhaps due to the rightly chosen parameters. The simulated transfer characteristics $I_D = f(V_{GS})$ of the TFT for different temperatures ranging from 300 to 400 K are shown in Figure IV-3 on linear (a) and logarithmic (b) scales.

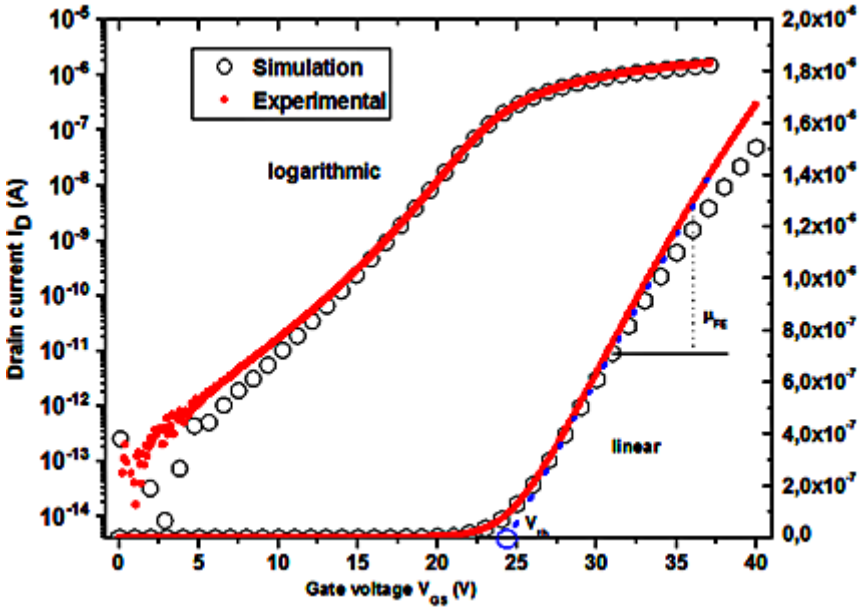


Figure IV-2:Experimental[122] and simulated transfer characteristics of pc-ZnO thin-film transistors.

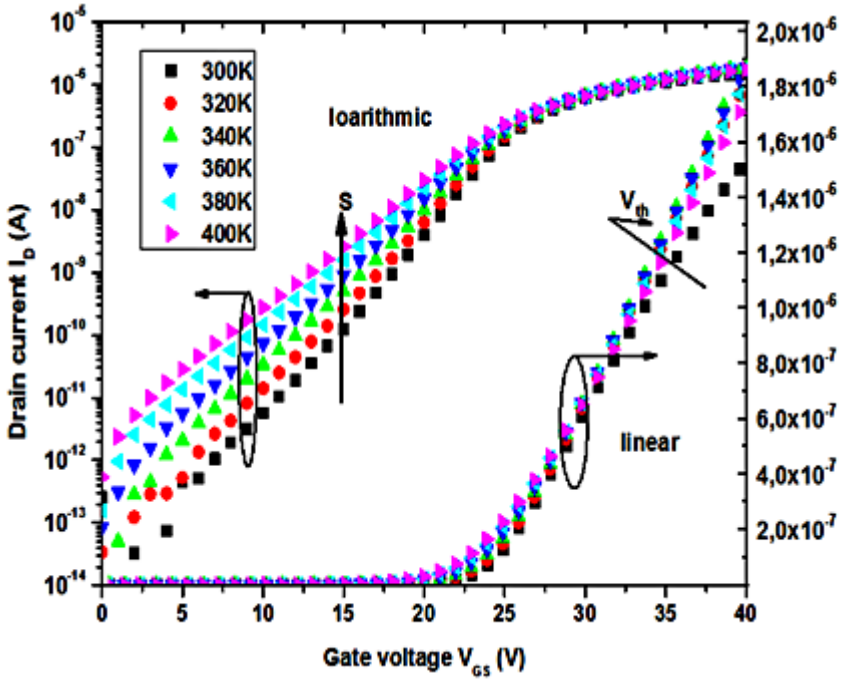
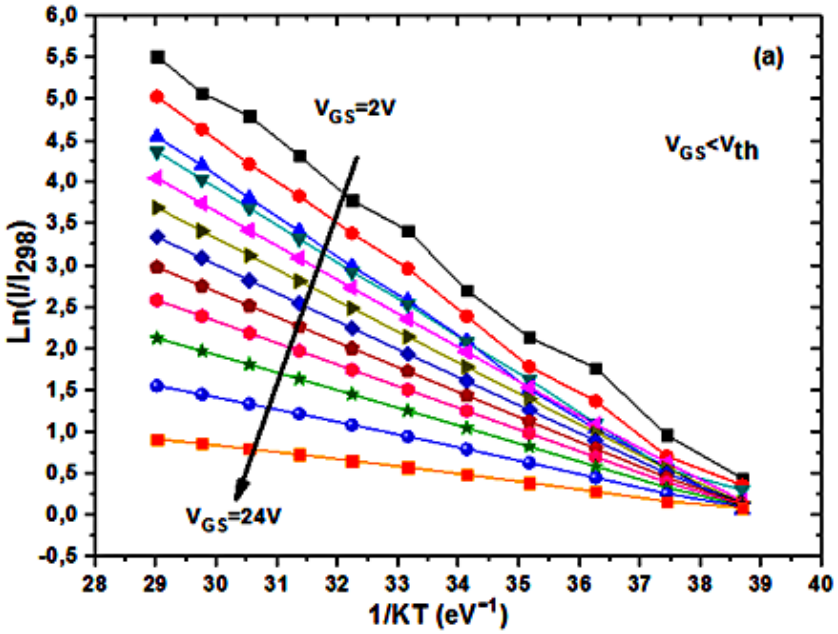
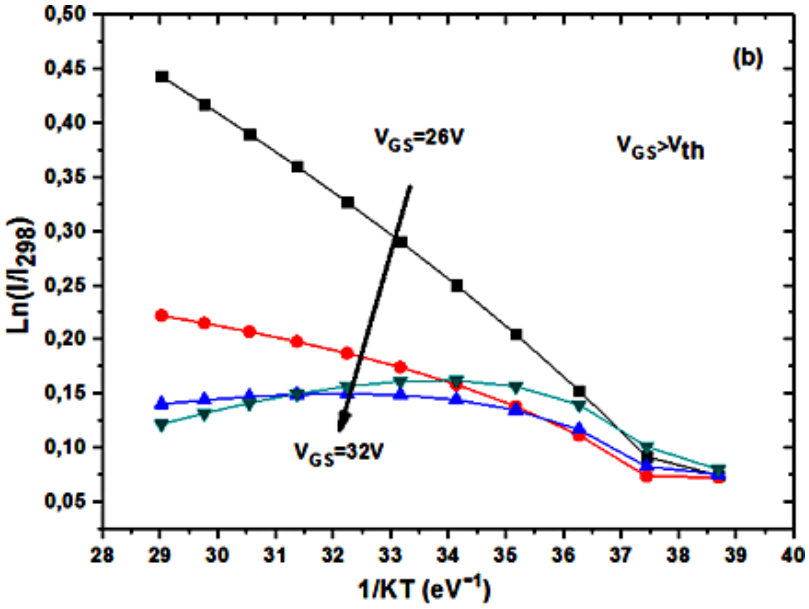


Figure IV-3:The simulated transfer characteristics $I_D = f(V_{GS})$ of the TFT for different temperatures ranging from 300 to 400 K on linear and logarithmic scales.

It is evident that the temperature has a different effect in the diverse regimes of the transfer characteristics. In the sub-threshold voltage, the temperature has a remarkable effect, that is it is thermally activated. On the other hand, it is not sensitive to temperature variation above the threshold voltage. Figure IV-4 presents the Arrhenius plot of the normalized current

I/I_{298} in the sub-threshold voltage (a), around the threshold voltage (b) and well above the threshold voltage (c). The current at 298 K I_{298} is evaluated by ATLAS in this work. These behaviours might be attributed to the ionization of the DOS and hence contribute to the enhancement of the number of electrons in the channel as the temperature increases in the sub-threshold voltage region. As the voltage nears its threshold, this enhancement is limited by the fact that electron accumulation in the channel of the TFT is saturated. It is also worth mentioning that beyond a threshold, the phenomenon is well reversed. This may be due to the complete contribution of the DOS as well as intrinsic electrons.





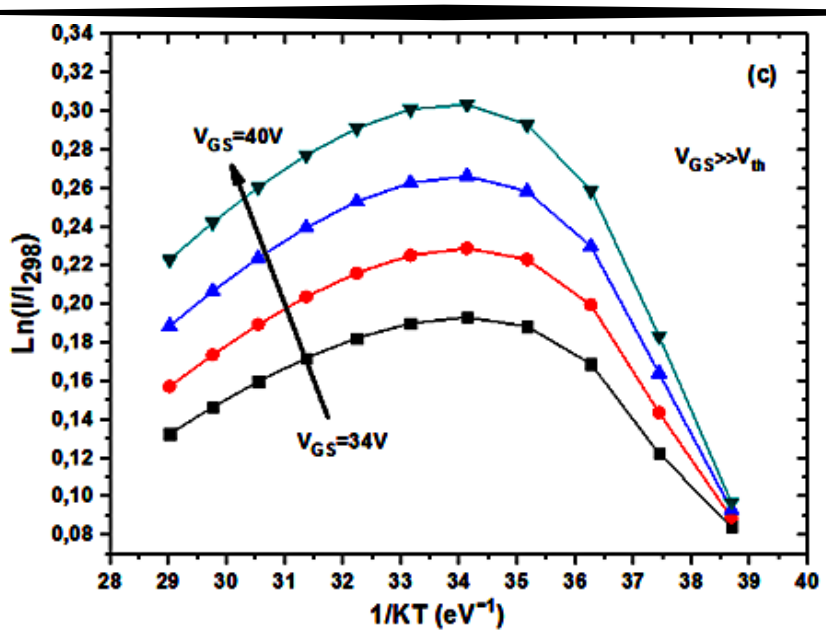


Figure IV-4:The Arrhenius plot of the normalized current I/I_{298}. (a) in the sub-threshold voltage, (b) just on the onset of the threshold voltage and (c) well beyond threshold voltage. I_{298} is the current at 298 K.

It is also clear that the activation energy is not the same in the varied segments of the characteristics. Figure IV-5 presents the activation energies of the current at different segments of the $I_D = f(V_{GS})$ transfer characteristics of the TFT. This activation energy versus gate voltage of ZnO TFT exhibits the same behavior as that in a-Si:H TFT [17].

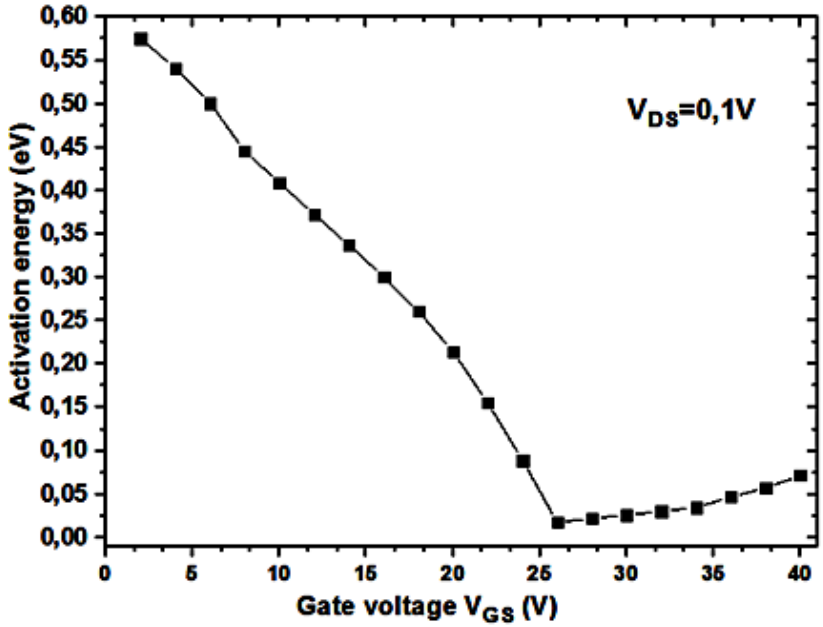


Figure IV-5:The evaluated activation energy versus the gate voltage.

The activation energy decreases with increasing gate voltage of the greatest value 0.57

eV at V_{GS}=2 V, which is close to the experimental results [17], to 0.019 eV at V_{GS}=26 V. Thereafter is a slight rise in Ea when limits 0.071 eV. The high values of the activation energy at low temperatures may be because to the fact that conduction mechanism is dominated by the intrinsic contribution. As the temperature increases the DOS contribution increases leading to a shallower activation energy.

The extracted field effect mobility and the threshold voltage from the transfer characteristics $I_D = f(V_{GS})$ of the pc-ZnO TFT for different temperatures are shown in Figure IV-6.

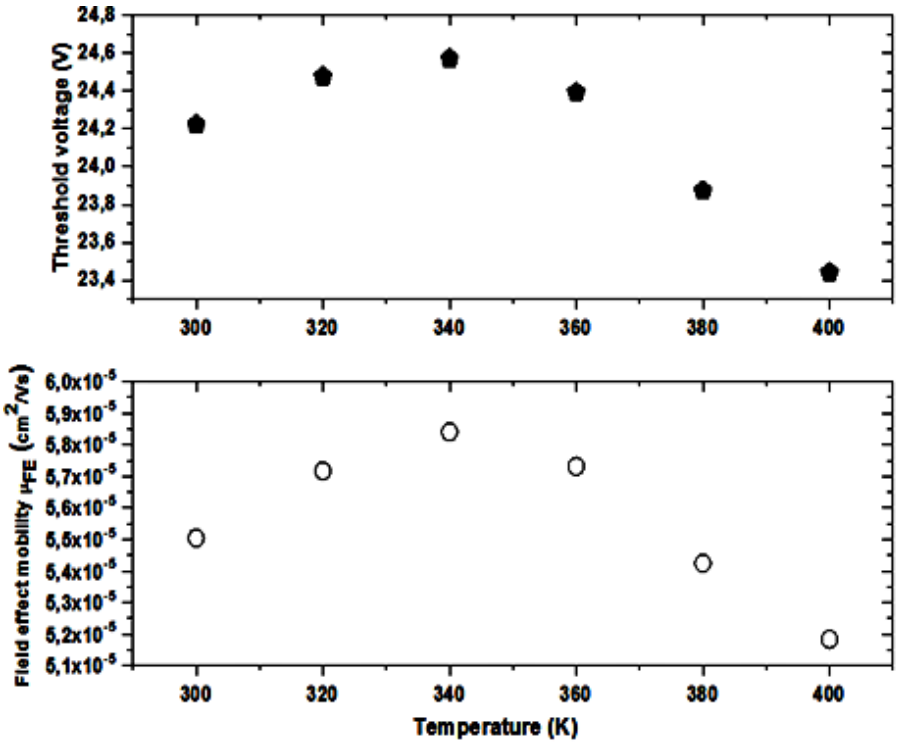


Figure IV-6:The effect of temperature on the field effect mobility and the threshold voltage of the pc-ZnO TFT.

The extracted field effect mobility (μ_{FE}) and the threshold voltage (V_{th}) from the transfer characteristics $I_D = f(V_{GS})$ are also temperature dependent. The mobility increments initially with increasing temperature; it then peaks before starting to decrease. This behavior may also be attributed to the contribution of the DOS to the electrons in the channel. At relatively low temperatures, the contribution of the DOS is negligible, which leads to the increase of the mobility. As the temperature increases; the contribution of the DOS rises leading to increasing collisions and hence a decrease in the mobility. Since the threshold voltage is proportional to the electric field mobility [18], it is expected that it follows the same pattern, which the case here.

IV.3 The effect of defects creation by optical stress on pc-ZnO thin film transistor at low temperature

IV.3.1 Modeling and simulation

In this section, modeling TFT at shape three dimensional cross- section of the pc-ZnO TFT structure used in this work is shown in Figure IV-7. The channel is 20 nm thick pc-ZnO, the substrate is a heavily doped n-type poly-silicon which also acts as a gate, the gate insulator is a 100 nm wide SiO_2 layer, the drain and source ohmic contacts are 5 µm long aluminum (Al). The separation between the source and drain is 30 µm. The width of the TFT is 180 µm.

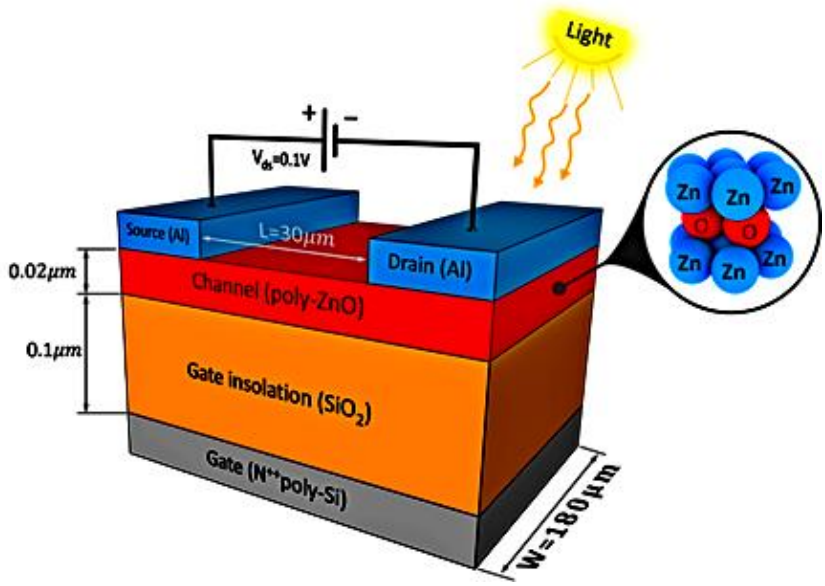


Figure IV-7:A three-dimensional view of the pc-ZnO TFT simulated in this work.

The channel is 20 nm thick pc-ZnO, the substrate is a heavily doped n-type poly-silicon which also acts as a gate, the gate insulator is a 100 nm thick SiO_2 layer, the drain and source ohmic contacts are made of aluminum (Al). The separation between the source and drain is 30 µm. The width of the device is 180 µm (not to scale).

A two-dimensional cross-section of the pc-ZnO TFT structure used in this work is shown in Figure IV-8 created by Tony Plot structure Silvaco. This represents the true dimensions of the studied TFT and observed. We note that the dimensions of source and drain very thin almost nonexistent. In order to get a good accumulation between the semiconductor and metal. This means excellent electrical conductivity for TFT.

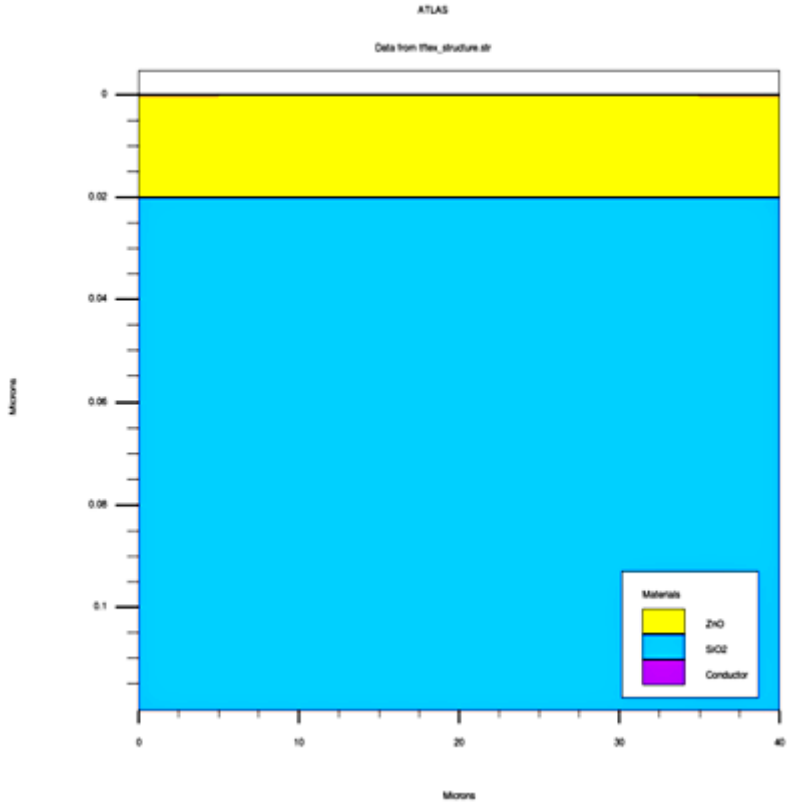


Figure IV-8:A Two-dimensional show the schematic cross section of the pc-ZnO TFT simulated by Atlas silvaco in this work.

This model relies on the utilization of Poisson's equation and the steady-state continuity equation, as described earlier. Through simulations, the electrical properties of the device are calculated by taking into account the specific physical structure and bias conditions. Of significant importance in this study is the computation of the current-voltage (I-V) characteristics associated with defects induced by illumination, with particular focus on the influence of stress optical effects. To facilitate these calculations, a set of specific parameters is employed, which are detailed in Table IV-2. Additionally, certain values are assumed for the schematic representation of the density of states (DOS) distribution. These assumptions allow for a better understanding and analysis of the behavior of the device within the context of this study.

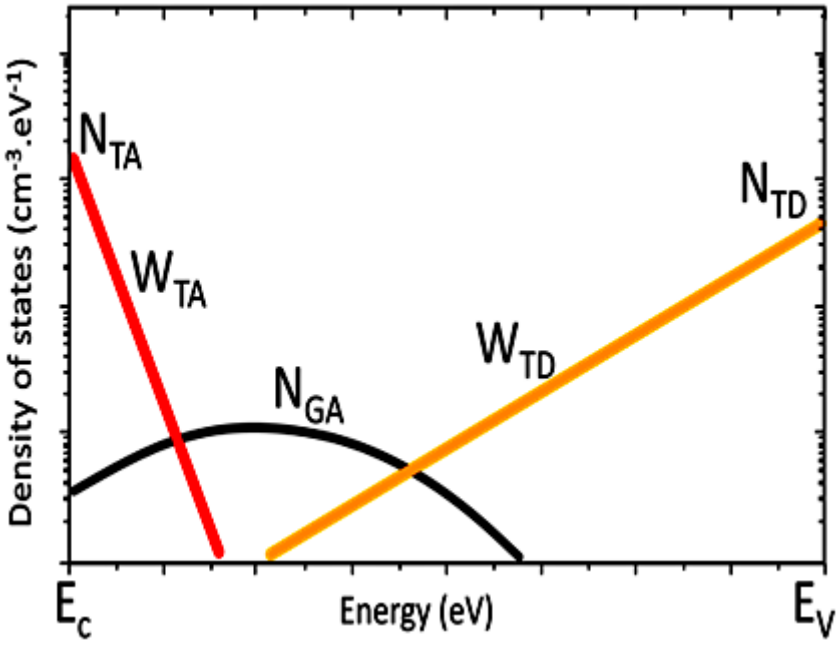


Figure IV-9:The schematic of DOS distribution.

Table IV-2:The parameters of the DOS model in pc-ZnO pre-illumination used in this study

Parameters	**Values**	**Ref**
Electron affinity	4.29 eV	[125]
Dielectric constant	8.12	[126]
Electron mobility	40 $cm^2/V.s$	[30]
Hole mobility	1.5 $cm^2/V.s$	[30]
Effective conduction band states	4.3×10^{18} cm^{-3}	[127]
Effective valence band states	4.3×10^{18} cm^{-3}	[127]
Energy gap at 300K	3.4 eV	[128]
Density of acceptor-like tail states	1.05×10^{21} $cm^{-3}.eV^{-1}$	[11]
Density of donor-like tail states	1.05×10^{19} $cm^{-3}.eV^{-1}$	[11]
Capture cross section of electron and hole states	4.0×10^{-15} cm^2	[9]
Characteristic decay energy acceptor-like tail states	0.05 eV	Assu
Characteristic decay energy donor-like tail states	0.1 eV	Assu

The values used in our study are based on established empirical research, providing us with reliable parameters to effectively model the thin-film transistor (TFT) using the Atlas Silvaco software. Additionally, when representing the density of states (DOS) distribution graphically, as shown in Figure IV-9, we make the assumption of a characteristic decay energy for the donor/acceptor-like tail states. This assumption allows us to better understand and analyze the behavior of the TFT device within the framework of our study.

IV.3.2 Edge of three main TFT operating regimes and their points

We can separate the TFT operation regimes to edge three main shows the Figure IV-10.

1. Poole-Frenkel emission regime (1): In this regime, the electric field in the channel becomes high enough to cause the emission of electrons from traps in the channel region (leakage current). The Poole-Frenkel emission regime is characterized by a non-linear relationship between the drain current and the gate voltage, this regime includes point (head of hump).

2. Subthreshold regime (2): In this regime, the gate voltage is below the threshold voltage (V_t) of the TFT, and the drain current is mainly determined by the charge carrier concentration in the channel. The subthreshold regime is characterized by an exponential relationship between the drain current and the gate voltage, this regime includes point (depth of well).

3. Above-threshold regime (3): In this regime, the gate voltage is above the threshold voltage of the TFT, and the drain current is mainly determined by the voltage applied to the gate. The above-threshold regime is characterized by a linear relationship between the drain current and the gate voltage, this regime includes point (saturation).

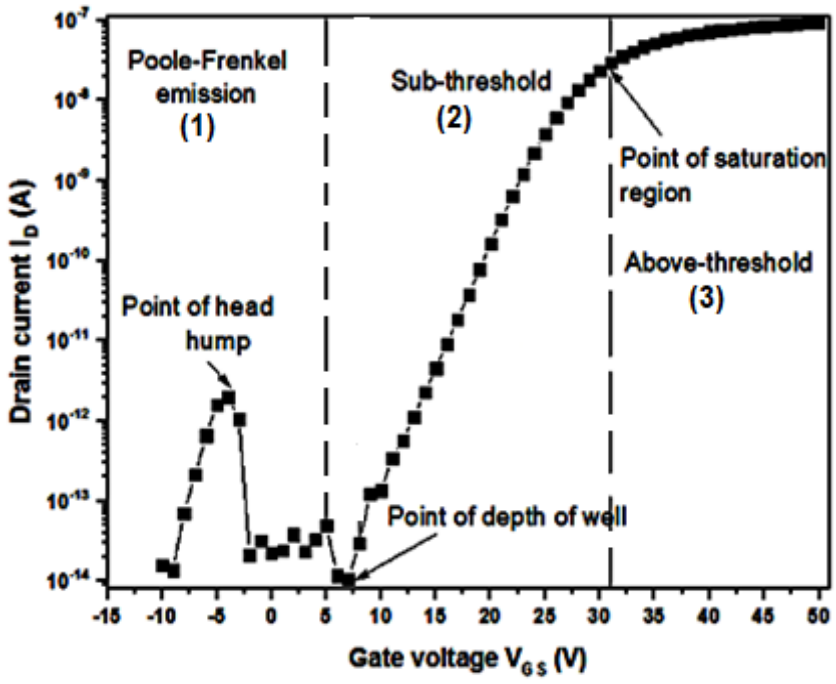


Figure IV-10:The simulated transfer characteristics ID = f(VGS) of the pc-ZnO TFT pre-illumination.

In our investigation of pc-ZnO TFTs, we observed distinct properties within each of the three operating systems, which have a profound effect on the electrical properties of the TFT. In the first system, referred to as the Poole-Frenkel emission system, the notable feature is the presence of a peak in the leakage current, known as the 'hump head'. This peak is attributed to the emission of the charge carriers over the energy barriers.

Turning to the second system, known as the subthreshold region, we define the deepest point within this region as the 'well depth', represented by Ioff. This point indicates the minimum level of current achieved when the TFT is in the off state. Going further, the third regime, called the subthreshold saturation zone, represents the transition from subthreshold to behaviors above the threshold. At this transition point, which is referred to as 'the saturation point' and denoted as the threshold voltage Vth, significant current flow is observed in the TFT.

IV.3.3 Effect electron mobility μe at pc-ZnO TFT

Firstly, we conducted simulation to investigate the influence of electron mobility (μe) on the current-voltage (I-V) characteristics of polycrystalline zinc oxide (pc-ZnO) thin-film transistors (TFTs). We systematically modified the electron mobility starting from its initial pre-illumination value of 40 m^2/Vs and increased it in increments of 10 m^2/Vs, ultimately reaching a final value of 90 m^2/Vs. Following each modification, we measured the I-V characteristics of the pc-ZnO TFT.

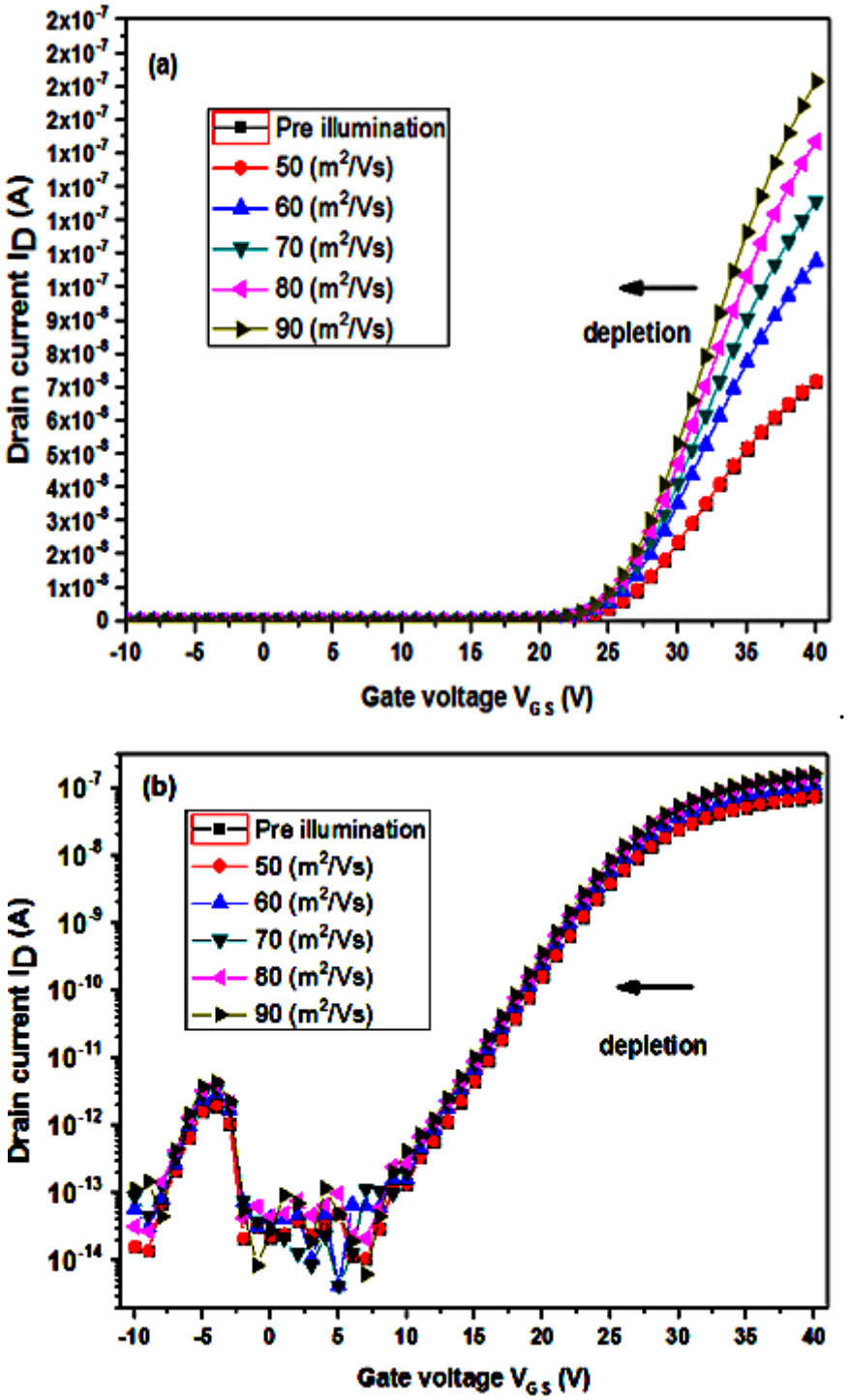


Figure IV-11:The simulated transfer characteristics ID=f(V_{GS}) of the TFT for different electron mobility ranging from 40 to 90 (cm^2/V.s) on linear (a) and logarithmic (b) scales.

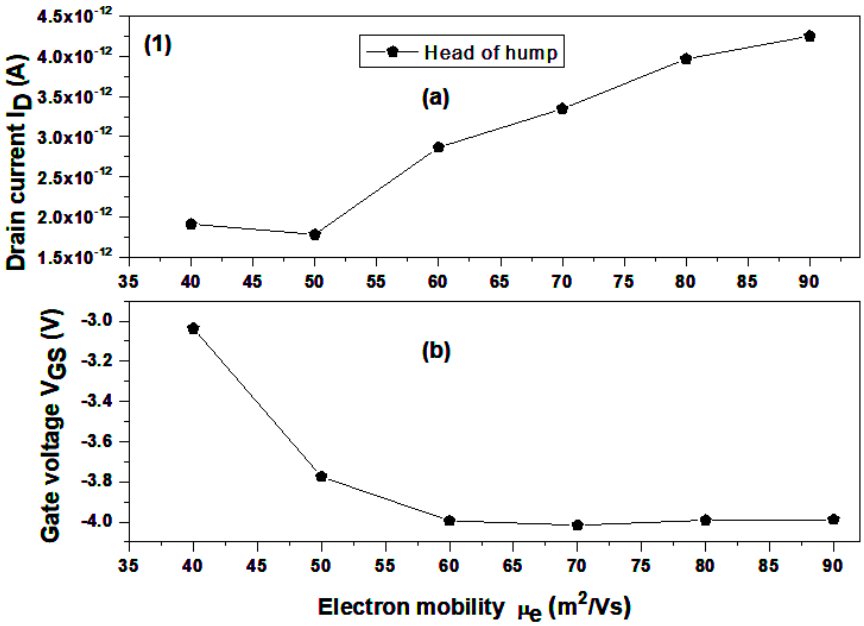
Our results revealed a significant impact of electron mobility on the accumulation of electrons within the device. As the electron mobility increased, the accumulation of electrons became more limited, leading to a reduction in current flow, as shown in Figure IV-11(b). Remarkably, we observed that the subthreshold region of the I-V curve was particularly

sensitive to changes in electron mobility. This finding suggests that electrons play a crucial role in influencing the electrical properties of the device, which determines the turn-on characteristics of the TFT.

IV.3.3.1 Effect electron mobility μ_e at the points

We have explored the impact of electron mobility on the transport properties of the polycrystalline zinc oxide (pc-ZnO) thin-film transistor (TFT) channel. When the device is exposed to light, there is an observed increase in the mobility of free electrons within the conduction band. To analyze the behavior of the TFT, we have examined the TFT curve and identified three distinct regions, each containing critical points that have a significant influence on the device's electrical properties.

Figure IV-12 illustrates our analysis, where we have compared different scenarios by examining the variations in drain current (I_{DS}) and gate voltage (V_{GS}) at these critical points with respect to changes in electron mobility. By conducting these comparisons, we have gained valuable insights into the relationship between electron mobility and the electrical characteristics of the pc-ZnO TFT. This investigation provides valuable information for understanding and optimizing the performance of the device in practical applications.



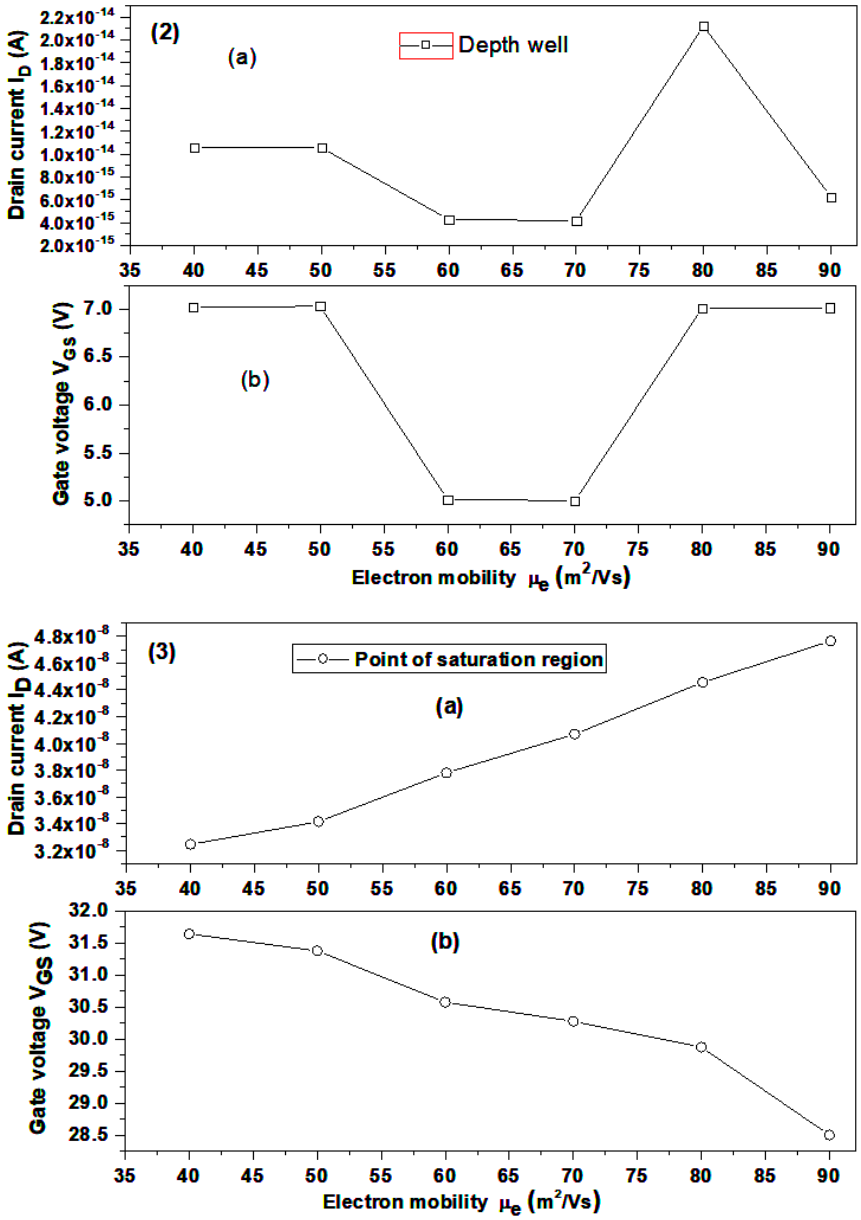


Figure IV-12: The effect of electron mobility on (1) Head of hump (2) Depth well (3) point of saturation drain current and the gate voltage extracted from the transfer characteristics $I_D=f(V_{GS})$.

We observed a correlation between the mobility of free electrons and the variations in drain current (I_{DS}) and gate voltage (V_{GS}) at curve (2) in point depth of well behavior current in the linear region (sub-threshold) of a thin-film transistor (TFT), the current exhibits a linear relationship with the applied voltage. This region is typically observed when the drain-source voltage is relatively low. In this operating mode, the TFT functions as a voltage-controlled resistor. The current flowing through the TFT follows Ohm's Law, which states that the current is directly proportional to the applied voltage. As the voltage increases, the current through the TFT also increases proportionally. This linear relationship between current and voltage allows

for precise control of the TFT's conductivity, making it suitable for applications where a linear response is required, such as in amplifiers or linear voltage regulators.

In two specific points in the curve, namely the head of the hump and the saturation point, we observed an inverse relationship between the drain current (I_{DS}) and the gate voltage (V_{GS}) with respect to the mobility of free electrons. As the gate voltage (V_{GS}) increased to its highest value, the drain current (I_{DS}) decreased, indicating the presence of a Zone Charge of Space (ZCS) or depletion region. This phenomenon is depicted in Figure IV-13.

When a negative gate voltage is applied, it generates an electric field in the gate dielectric layer, attracting positively charged carriers (holes) to the interface between the gate dielectric and the channel material. Consequently, a depletion region forms in the channel material near the gate dielectric, resulting in a reduction in carrier concentration and an increase in channel resistance. This behavior has important implications for the electrical characteristics and performance of the device.

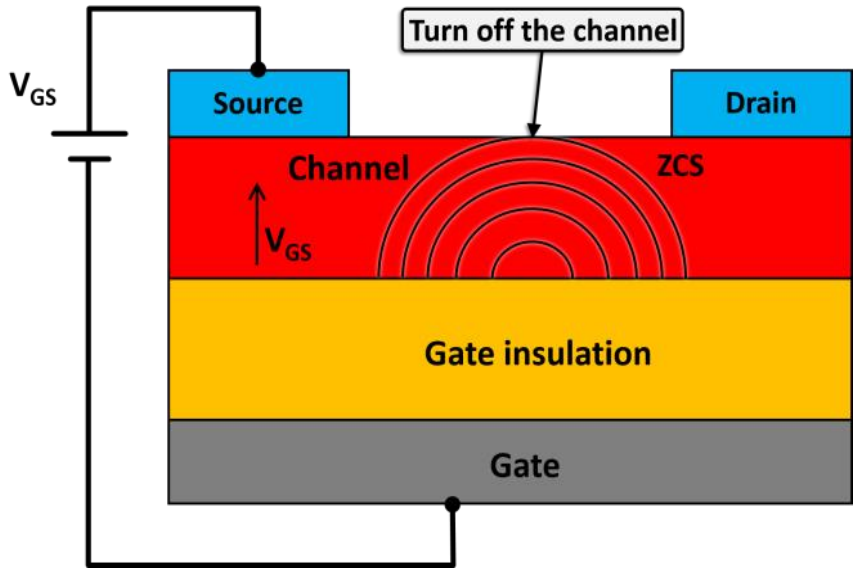


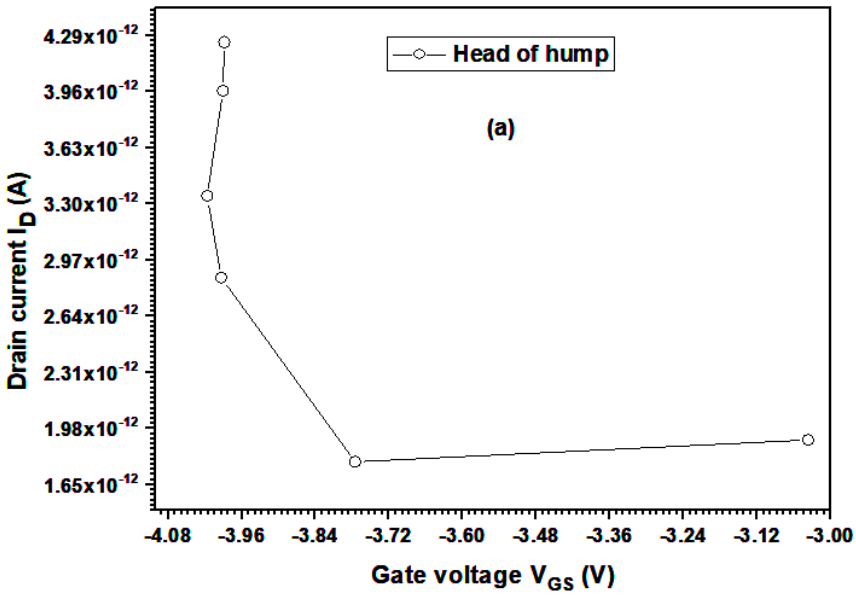
Figure IV-13:Mechanism of depletion region in TFT.

As the applied gate-source voltage (V_{GS}) is increased, the depletion region widens. This channel narrowing impedes the movement of electrons, eventually causing the transistor to turn off. The well depth (Ioff) on the curve corresponds to the off-state characteristics of the n-channel a-Si:H TFT, which describes its leakage current behavior under negative gate bias. Several leakage current mechanisms have been identified, including leakage through the a-SiNx:H gate dielectric, bulk conduction through the a-Si:H film, back-channel electron

conduction, and front channel hole conduction [27,28]. We expect similar mechanisms to be present in the pc-ZnO/SiO_2 TFT. The increase in drain current (I_{DS}) with increasing V_{GS} is in line with the electron mobility, indicating that the transistor is normally off. However, when V_{GS} is further increased, except at 90 (cm^2/Vs), there is a notable rise in the number of electrons, leading to a leakage current phenomenon.

IV.3.3.2 Topical survey of the points in log transfer characteristics

In this topical survey, we examine the key points in the logarithmic transfer characteristics of the thin-film transistor (TFT) and their response to light. By analyzing the curve of the TFT's logarithmic transfer characteristics, $I_D=f(V_{GS})$, we identify three important points. The point at the head of hump, observed under negative bias, corresponds to the contribution of Pool-Franck emission. The depth of well point represents a lower value of the drain current, which we interpret as the off-state current (Ioff). The saturation point, separating the sub-threshold and above-threshold regions as shown in Figure IV-10, exhibits minimal variation as V_{GS} increases. The drain current in this region remains relatively constant and is referred to as the saturation current (Ion). The sub-threshold slope (SS) is calculated as the inverse of the slope of the straight line connecting the saturation point and the well depth point. Additionally, the Ion/Ioff ratio is defined as the ratio of the current in the saturation region to the leakage current, extracted from the $I_D=f(V_{GS})$ characteristic plotted on a logarithmic scale. Generally, topical survey the points the purpose of which is to study the effects (doping temperature, lighting, etc.) as well as the operation of TFT.



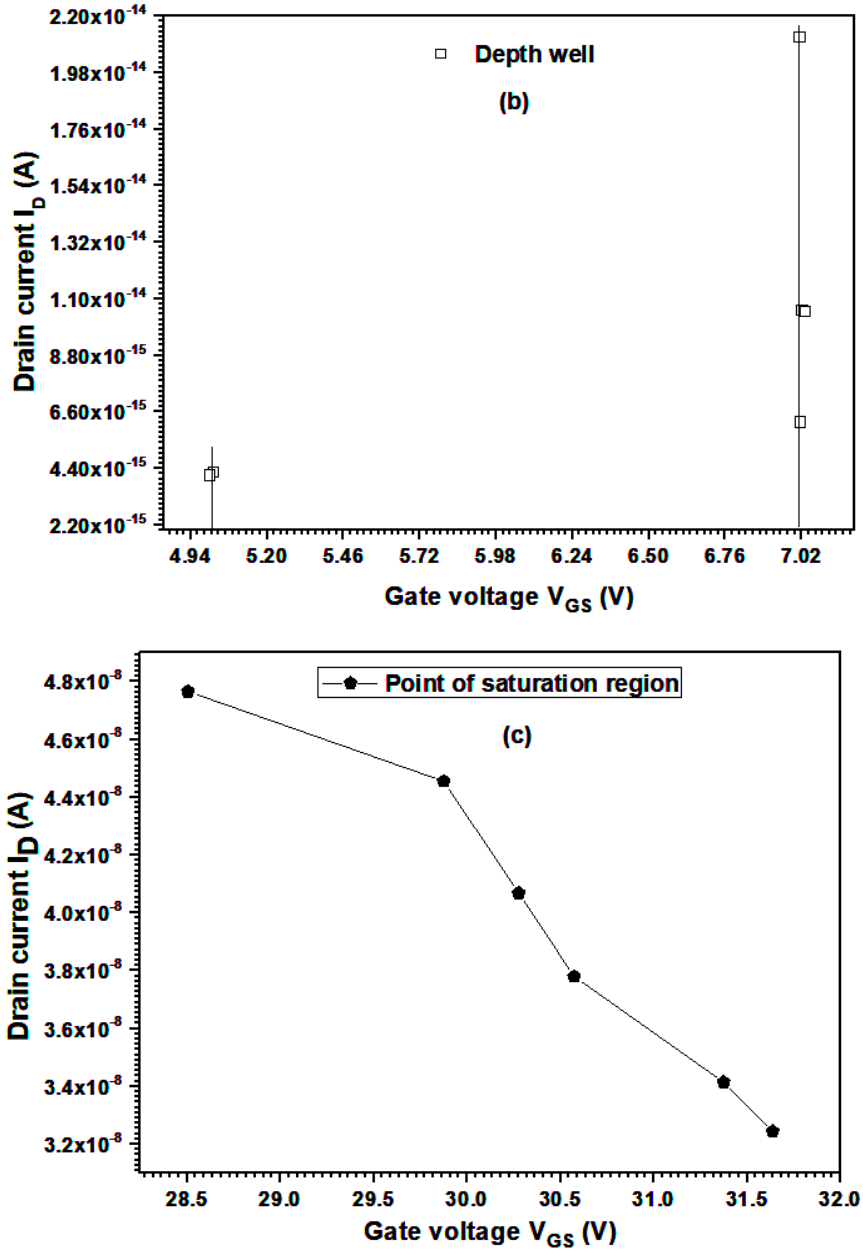
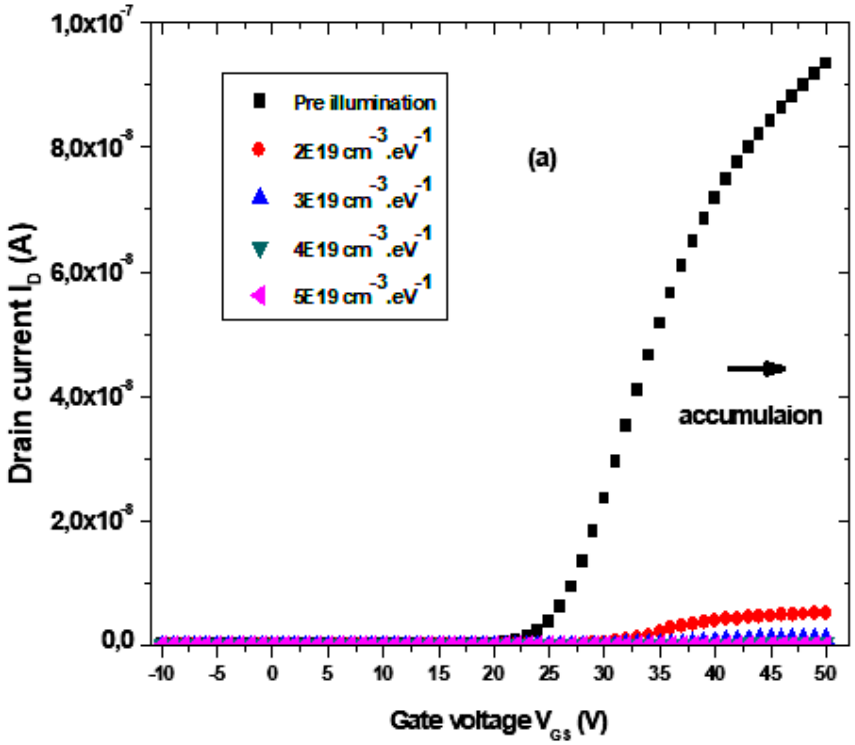


Figure IV-14:Position the points in log transfer characteristics $I_D=f(V_{GS})$.(a) Head of hump (b) Depth well (c) Point of saturation.

We found that the points at the head of hump appeared within the range of V_{GS} [-4, -3V], corresponding to I_D values between 1.7×10^{-12} and 4.3×10^{-12}A. Notably, at V_{GS}=-4V, we observed a relatively stable trend for most points, with an increase in I_D. Regarding the depth well points, they were observed at V_{GS} values ranging from 5 to 7.2V, with corresponding I_D values between 1.7×10^{-14} and 1.75×10^{-14}A. Specifically, three points were located at V_{GS}=5V, while the remaining points were at V_{GS}=7.2V. The saturation point exhibited a uniform change along a straight line, starting from V_{GS}=28.5V and $I_D=4.75\times10^{-8}$A, and ending at V_{GS}=31.65V and $I_D=3.23\times10^{-8}$A.

IV.3.4 Effect of donor-like tail states at pc-ZnO TFT

We varied the density of donor-like tail states in the range of 1 to 5 10^{19} ($cm^{-3}.eV^{-1}$) during pre-illumination. The transfer characteristics of the pc-ZnO TFT, which describe the relationship between the gate voltage and the drain current, showed a significant sensitivity to variations in the donor-like tail states. This means that even small changes in the DOS had a noticeable impact on the electrical behavior of the TFT. The reason for this sensitivity can be attributed to the fact that the semiconductor material used in the TFT's channel, known as the active layer, had a poly-crystalline structure.



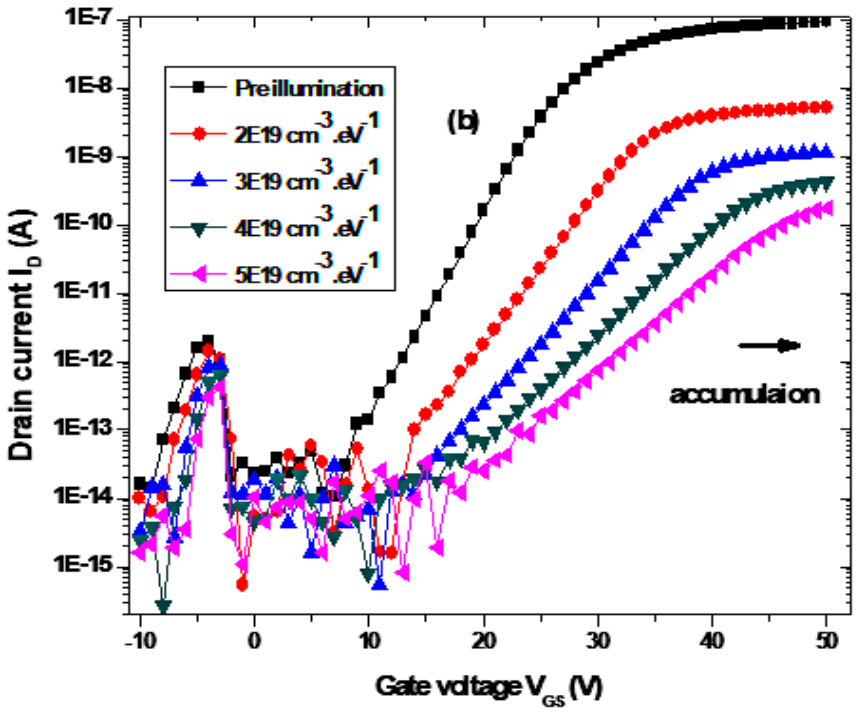


Figure IV-15:The simulated transfer characteristics $I_D=f(V_{GS})$ of the TFT for different density of donor-like tail states ranging from 1 to 5×10^{19} ($cm^{-3}.eV^{-1}$) on linear (a) and logarithmic (b) scales.

In poly-crystalline materials, the presence of grain boundaries and defects can significantly affect the transport of charge carriers, leading to variations in the device's electrical properties. Hence, changes in the DOS of the pc-ZnO TFT had a direct influence on its transfer characteristics. Initially, there was a significant impact on the transfer characteristics as the DOS increased, but eventually, the effects stabilized as the DOS reached higher values. This observation is clearly depicted in the linear curve of the transfer characteristics. Moreover, the specific points on the curve exhibited significant changes, as evident from the logarithmic curve shown in Figure IV-15. Interestingly, we observed that while the electron mobility influenced the left side of the sub-threshold slope curve during pre-illumination, the donor-like tail states had a more pronounced effect on the right side of the curve, despite having the same charge nature.

IV.3.4.1 Effect of donor-like tail states at the points

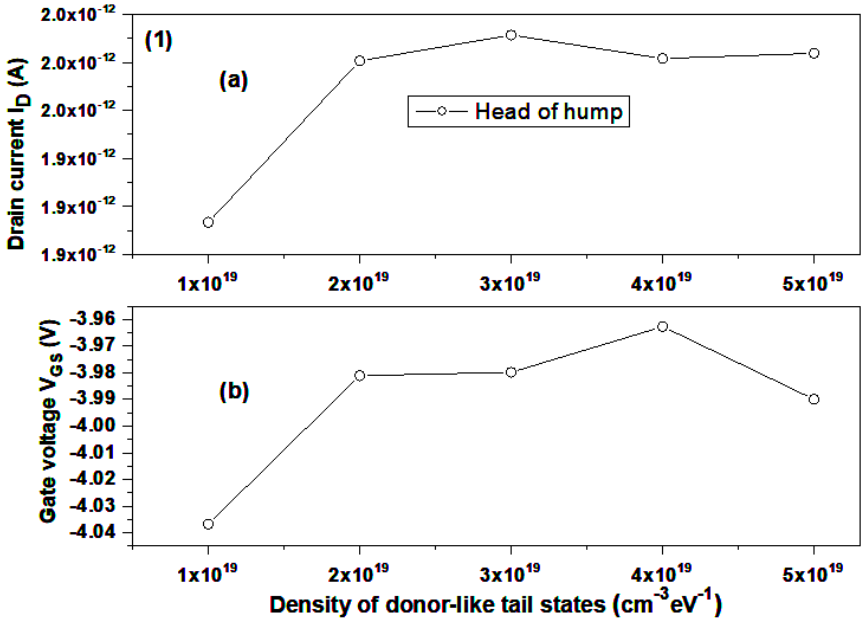
Donor-like tail states can have different effects on the electrical properties of a thin-film transistor (TFT) depending on their location within the device. Here are the effects of donor-like tail states at three different points in a TFT:

- Head of hump (leakage current): At the head of the hump in a TFT, donor-like

tail states can lead to an increase in the leakage current. This is because the tail states act as traps for electrons, which can accumulate at the interface between the gate dielectric and the semiconductor channel.

- Depth of the well (cut current): At the depth of well in a TFT, donor-like tail states can increase the cut-off current. The cut-off current is the current that flows through the device when the gate voltage is below the threshold voltage. Donor-like tail states can increase the density of trap states in the semiconductor channel, which can lower the energy barrier for electron tunneling and increase the cut-off current.

- Point of saturation (on current): At the point of saturation in a TFT, donor-like tail states can affect the on-current. The on-current is the current that flows through the device when the gate voltage is above the threshold voltage. Donor-like tail states can increase the density of charge carriers in the semiconductor channel, which can increase the on-current. However, if the tail states are too close to the conduction band edge, they can also act as traps for the charge carriers, reducing the effective mobility and leading to a decrease in the on-current.



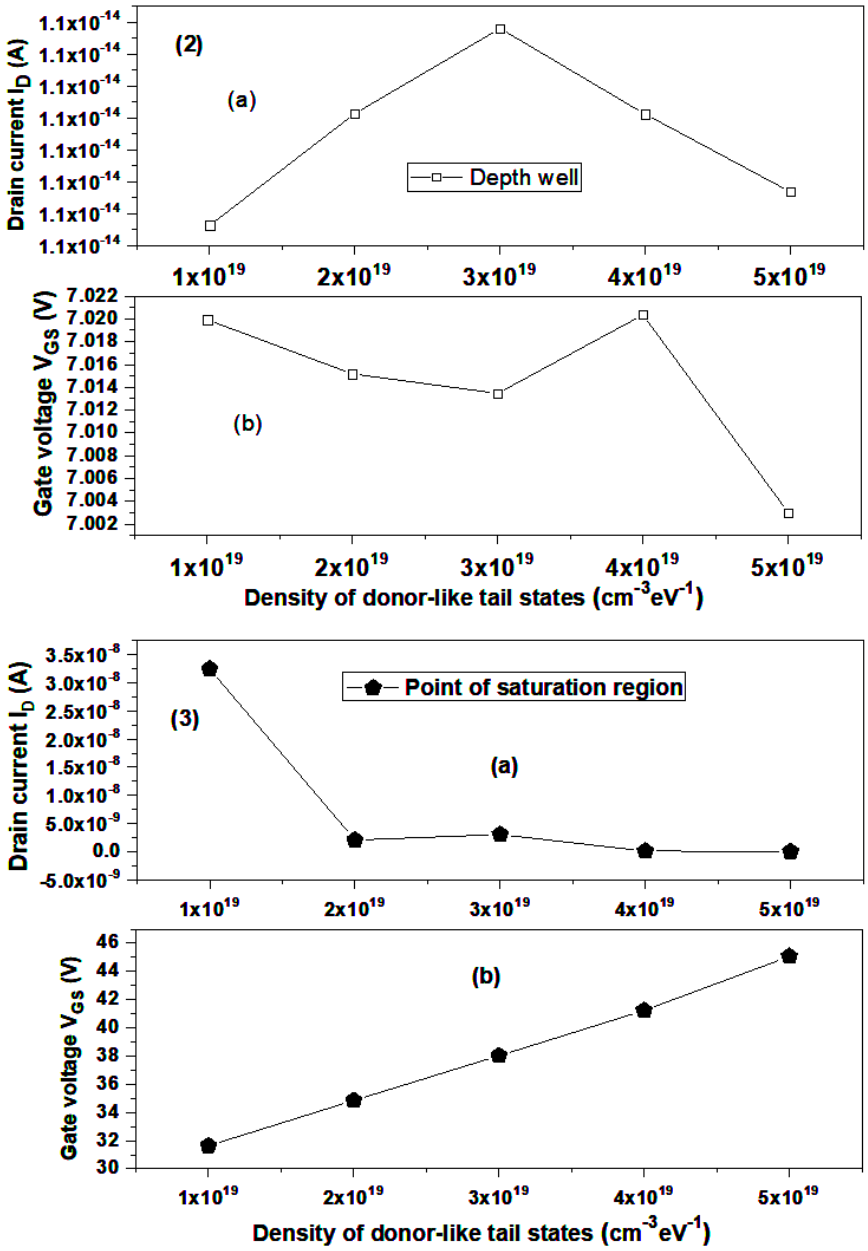


Figure IV-16:The effect of electron mobility on (1) Head of hump (2) Depth well (3) Point of saturation, the drain current and gate voltage extracted from the transfer characteristics $I_D=f(V_{GS})$ of Figure IV-15.

We assume the same previous explanations apply to the case density of donor-like tail states. To see the compatibility and the difference (I_{DS} and V_{GS}) between the two cases, we do a table in underneath.

Table IV-3:The difference (I_{DS} vs V_{GS}) between the two cases mobility and DOS.

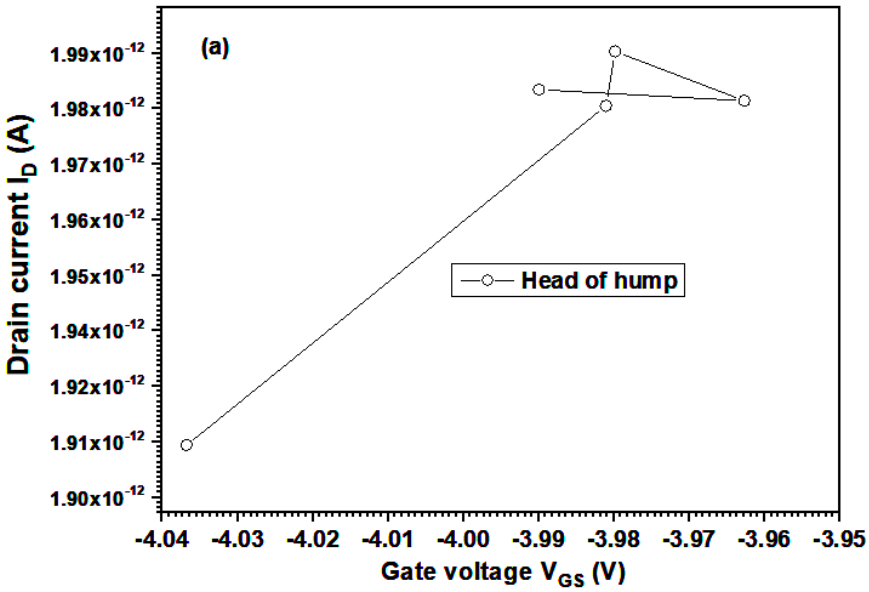
The cases	Mobility of electron	donor-like tail states
Head of hump	Inversion	Consensus
Deap of well	Consensus	Inversion
Point of saturation	Inversion	Steady

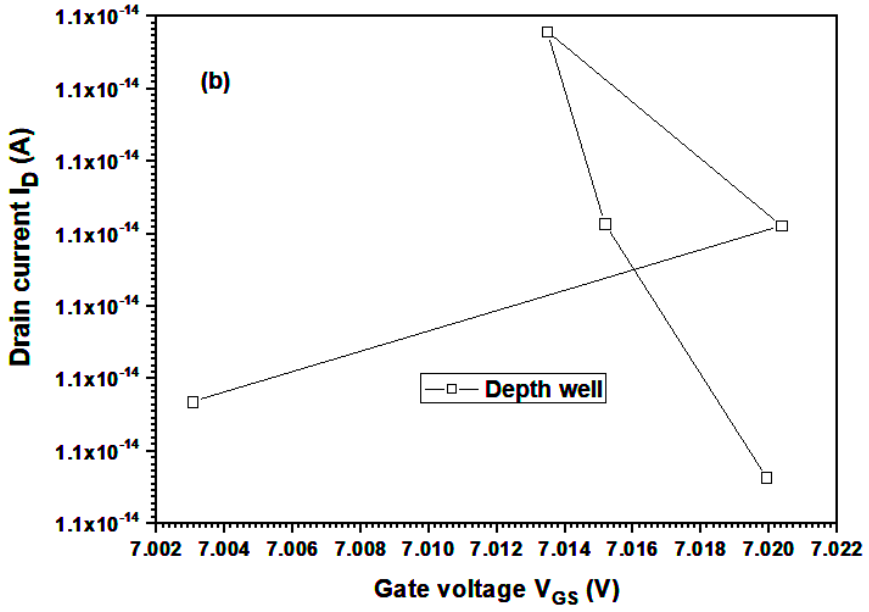
We observed that the impact of donor-like tail states at (I_{DS} vs V_{GS}) on the leakage current (head of hump) and the current in the depth well (off state) exhibits an opposite trend compared to the effect of electron mobility. Specifically, when considering the DOS, the leakage current demonstrates behavior similar to the current in the saturation region, while in the case of electron mobility, it resembles the behavior of the current in the linear region. This implies that the presence of defects in the DOS has a distinct effect on the electrical characteristics of the system, leading to variations in the leakage current and the off-state current depending on the DOS. These findings highlight the contrasting influences of DOS and electron mobility on the performance of the device, as explained in the previous discussion.

In the case of the saturation point, it is observed that the current reaches the saturation state (Steady) rapidly when considering the donor-like tail states (DOS), as the pc-ZnO TFT operates in the accumulation state. This indicates that the TFT quickly stabilizes its current behavior in response to the applied voltage. Conversely, when considering the electron mobility state in which the device operates in the depletion state, it takes a longer time for the current to reach saturation. This suggests that the electron mobility state exhibits a slower response and requires a longer duration to achieve a steady-state current. The difference in the saturation behavior between the DOS and electron mobility states underscores the contrasting characteristics and dynamics of these two factors in influencing the performance of the pc-ZnO TFT.

IV.3.4.2 Topical survey of the points in log transfer characteristics

Results for donor-like tail states are as follows:


(a)
Drain current I_D (A)
1.99x10^{-12}
1.98x10^{-12}
1.97x10^{-12}
1.96x10^{-12}
1.95x10^{-12}
1.94x10^{-12}
1.92x10^{-12}
1.91x10^{-12}
1.90x10^{-12}
Head of hump
-4.04 -4.03 -4.02 -4.01 -4.00 -3.99 -3.98 -3.97 -3.96 -3.95
Gate voltage V_{GS} (V)


(b)
Drain current I_D (A)
1.1x10^{-14}
Depth well
7.002 7.004 7.006 7.008 7.010 7.012 7.014 7.016 7.018 7.020 7.022
Gate voltage V_{GS} (V)

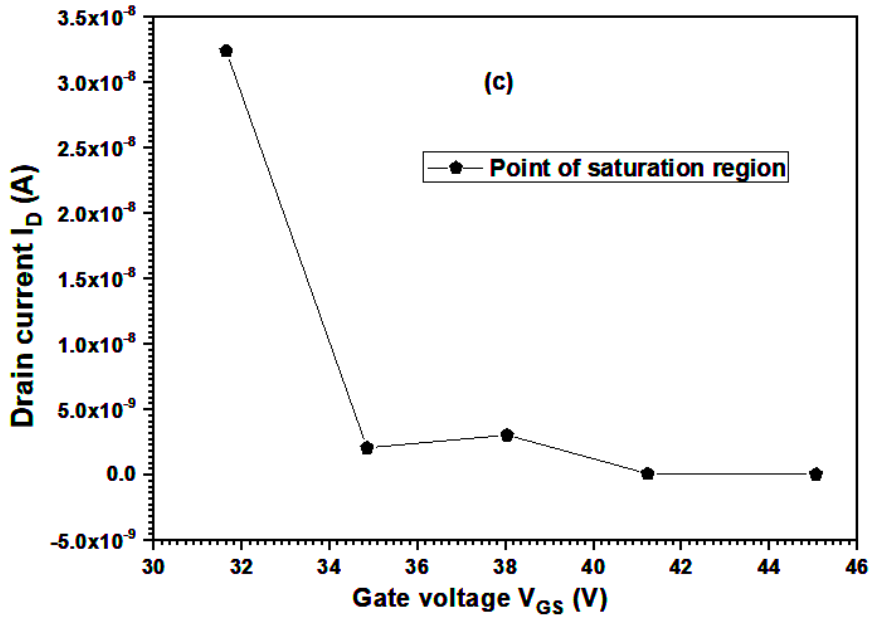
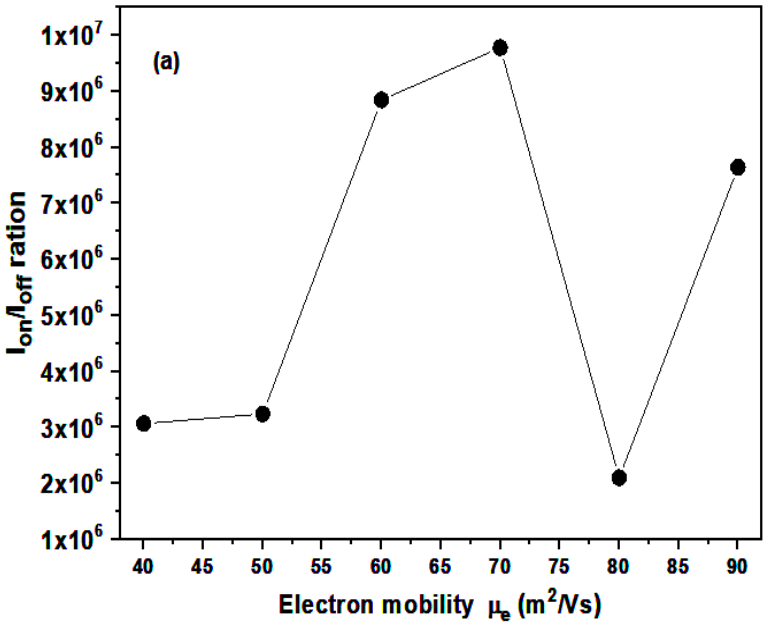

(c)
Drain current I_D (A)
3.5x10^{-8}
3.0x10^{-8}
2.5x10^{-8}
2.0x10^{-8}
1.5x10^{-8}
1.0x10^{-8}
5.0x10^{-9}
0.0
-5.0x10^{-9}
Point of saturation region
30 32 34 36 38 40 42 44 46
Gate voltage V_{GS} (V)

Figure IV-17:Position the points in log transfer characteristics $I_D=f(V_{GS})$.(a) Head of hump (b) Depth well (c) Point of saturation.

We observed that the points at the heads of the hump in the transfer characteristics of the device corresponded to a gate-source voltage (V_{GS}) range of [-4.04, -3.96V], with drain current (I_D) values ranging from [1.91×10^{-13}, 1.98×10^{-13}A]. In the region representing the depth well, the V_{GS} range was [7, 7.02V], with a very small increment of 0.01V, and the corresponding I_D values ranged from [1.05×10^{-14}, 1.069×10^{-14}A]. Interestingly, the change in V_{GS} had a similar effect on the gate-source current. However, in terms of mobility, the behavior of the saturation region varied irregularly. In this region, the V_{GS} range was observed to be between [31.6, 45V], with I_D values ranging from [1.88×10^{-10}, 3.245×10^{-8}A]. For most points, there was a consistent I_D value of approximately 3.245×10^{-8}A as V_{GS} increased.

IV.3.5 Calculation of Ion/Ioff ration and SS of pc-ZnO TFT

Through careful observation and analysis of the transport characteristics of polycrystalline zinc oxide (pc-ZnO) thin-film transistor (pc-ZnO) (TFT), valuable insights can be gained regarding its electrical properties, including its sub-threshold and Ion/Ioff ratio. By carefully selecting specific points along the log transfer characteristic curve, the $I_D = f(V_{GS})$ associated with the TFT can be determined. The results obtained from these analyzes allow an efficient assessment and evaluation of TFT performance, taking advantage of the three points identified in the transport characteristics.



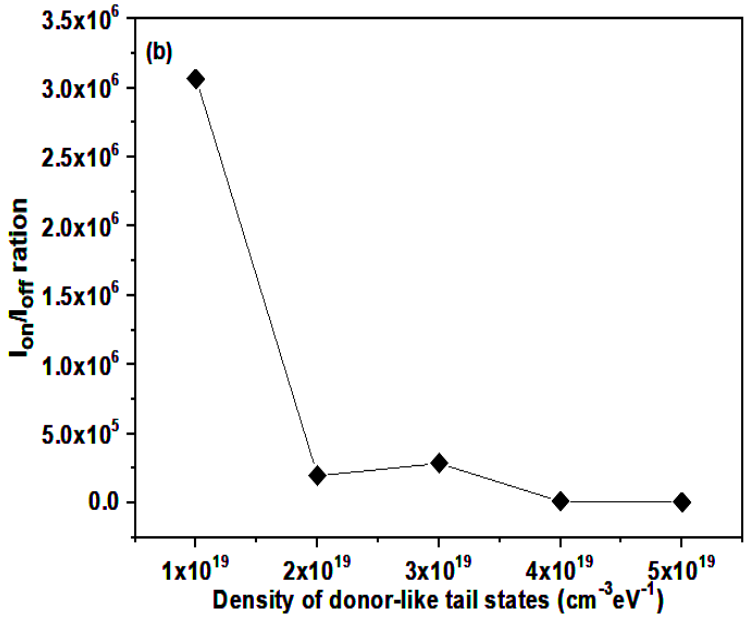
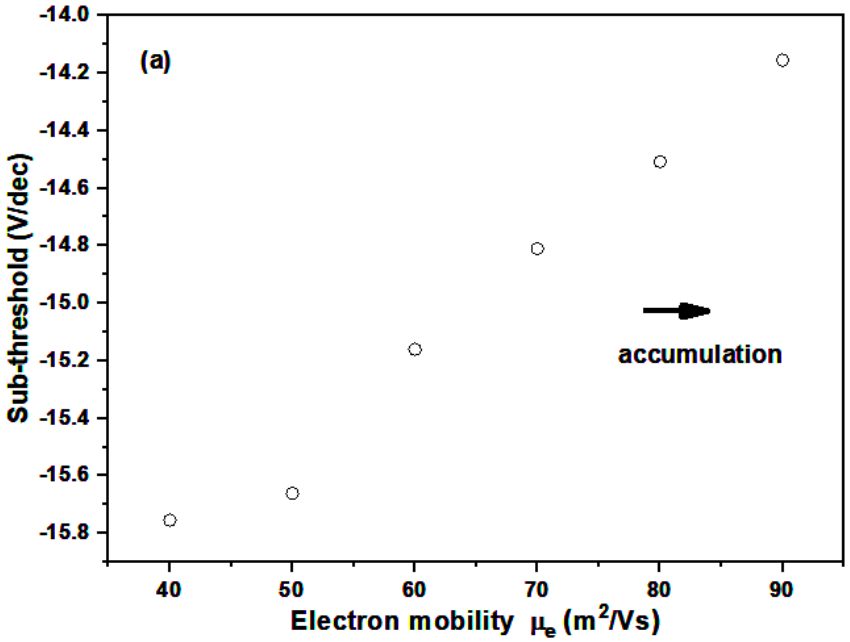


Figure IV-18:Curve I_{on}/I_{off} ration for the effect of (a) the electron mobility (b) the density of donors-like tail states.

We show of the Figure IV-18. (a) It's unstable in the field 10^6 to 10^7. (b) At first, it's at the highest value at 10^6 then steady at 10^5 in other values.



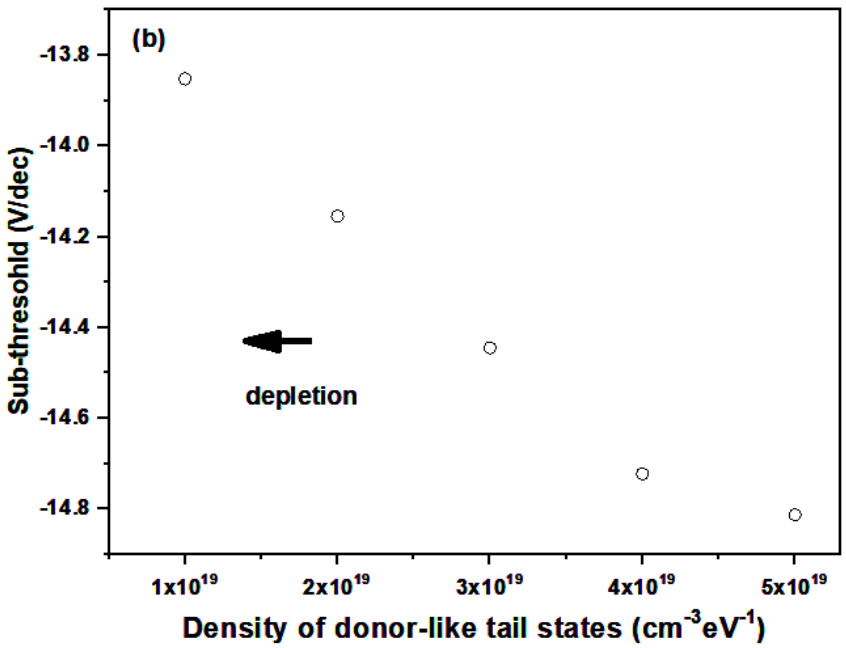


Figure IV-19:Curve Sub-threshold for the effect of (a) the electron mobility (b) the density of donor-like tail states.

The sub-threshold values (SS) obtained in both cases exhibit negative values ranging from -14 to -16 V/decade. Interestingly, there is a consistent pattern of SS changing uniformly towards the right side, indicating that the TFT is transitioning to an accumulation state. Conversely, the transformation observed in the density of donor-like states suggests a shift towards depletion, manifesting as a leftward shift. Notably, when comparing the direction of sub-threshold (SS) changes with the transfer characteristics $I_D=f(V_{GS})$ of the TFT, we observe a contradictory relationship between the two. Clarified, we can write equation (II-13) as follows:

$$SS = \left(\frac{\Delta(logI_{DS})}{\Delta V_{GS}}\right)^{-1} \qquad (IV\text{-}3)$$

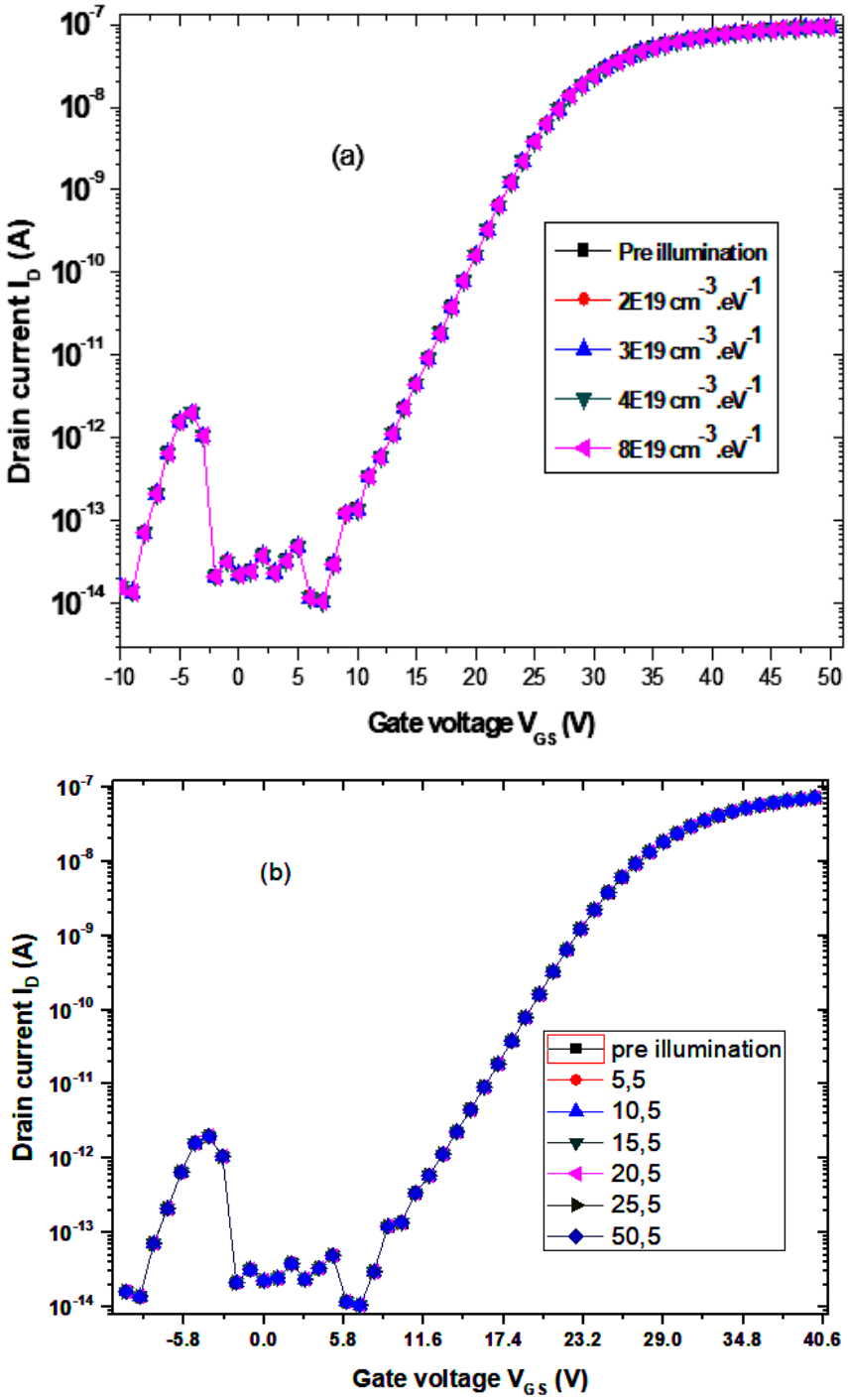


Figure IV-20:The simulated logarithmic transfer characteristics $I_D=f(V_{GS})$ of the TFT for different hole mobility (a) and for different density of acceptor-like tail states (b) scales.

The transfer characteristics of a thin-film transistor (TFT) refer to the relationship between the gate voltage and the drain current. In the case of polycrystalline ZnO TFTs, it is observed that there is no significant effect on the transfer characteristics. This lack of effect can be attributed mainly to the low-temperature behavior of ZnO [131], as well as the intrinsic nature of ZnO as an n-type semiconductor.

One reason for the negligible impact on the transfer characteristics is the low-temperature effect. ZnO TFTs typically operate at relatively low temperatures during their fabrication and operation. At these lower temperatures, the electrical properties of ZnO, including carrier mobility and conductivity, can be influenced. The low-temperature behavior of ZnO may contribute to a more stable and consistent transfer characteristic response, resulting in minimal variations. Another factor is the intrinsic nature of ZnO as an n-type semiconductor. ZnO exhibits an abundance of free electrons, making it an n-type material. In an n-type semiconductor, the transfer characteristics are primarily determined by the behavior of the majority charge carriers, which are electrons in this case. The electron mobility and concentration in ZnO can be relatively high, contributing to a consistent and predictable response in the transfer characteristics.

The combination of the low-temperature behavior of ZnO and its n-type nature results in minimal variations in the transfer characteristics of polycrystalline ZnO TFTs. While other factors such as device geometry, material quality, and processing conditions can still affect the TFT performance, the inherent properties of ZnO contribute to the observed stability in the transfer characteristics.

IV.4 The effects nano-grain size and boundary on nc-ZnO TFT related to deposition temperature

IV.4.1 Characterization and Fabrication of nc-ZnO TFT

The chemical compositions of thin films grown are obtained by x-ray photoelectron spectroscopy measurements (XPS; Thermo K-Alpha monochromated high-performance XPS spectrometer). XPS survey scans of ZnO films grown at different deposition temperatures by ALD technique are plotted in Figure IV-21.

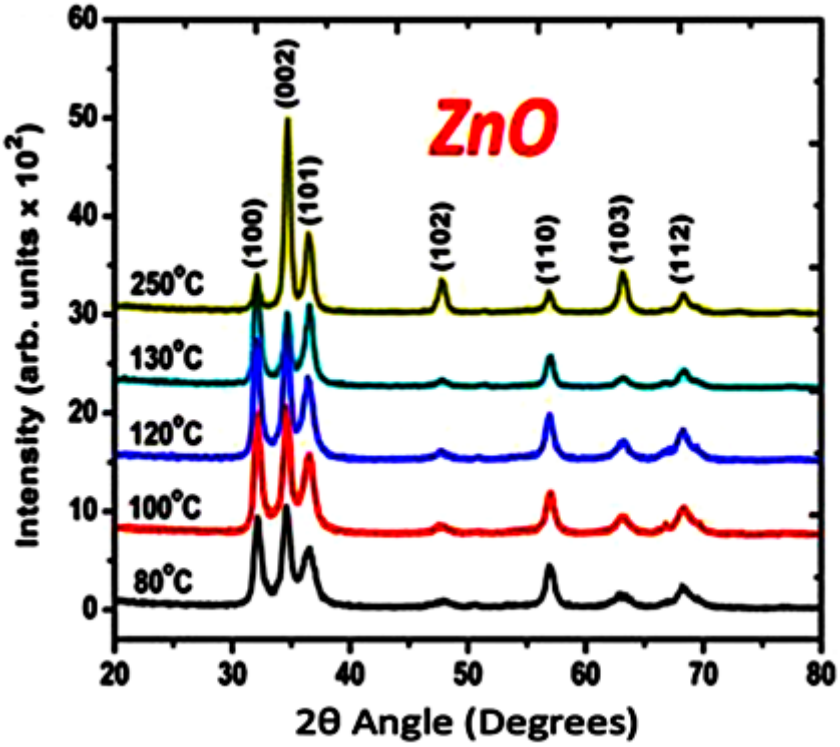


Figure IV-21:Measured x-ray diffraction patterns of nano ZnO films deposited at different temperatures [132].

The XRD results show that ZnO films have a hexagonal wurtzite crystal structure, with no preferred orientation at low growth temperatures. At the highest growth temperature of 250 °C, the intensity of the (002) peak increases significantly. The diffraction maxima occurred at (100), (002) and (101) crystallographic orientations for all ZnO films.

The average crystallite size (D) of the ZnO grains from the XRD (Figure IV-21) patterns is calculated using the Scherrer relationship [14]:

$$D = \frac{K\lambda}{\beta \cos\theta} \qquad (IV\text{-}2)$$

Where the constant K = 0.9, β is the full-width at half maximum of the diffraction peak and θ is the corresponding Bragg's angle of reflection from the (hkl) planes. λ is the wavelength of the x-rays. The diffractometer used for the characterization of our samples is (XPS; Thermo K-Alpha monochromated high-performance XPS spectrometer) with Aluminium anode having an X-ray beam of wavelength Kα (Al). Besides they can be counted from the equation for photon energy is:

$$\lambda_{Al(K_\alpha)} = \frac{h.c}{E_{AlK\alpha}} \qquad (IV\text{-}3)$$

Where h is the Planck constant, c is the speed of light in vacuum and $E_{AlK\alpha}$=1486.7 (eV) is photon energy [15]. Altogether $\lambda_{AlK\alpha}$=8.3386Å. The average crystallite size as estimated from the diffraction peak corresponds to the reflection every seven planes using equation (1), at a temperature of 100℃ is~86.5 nm.

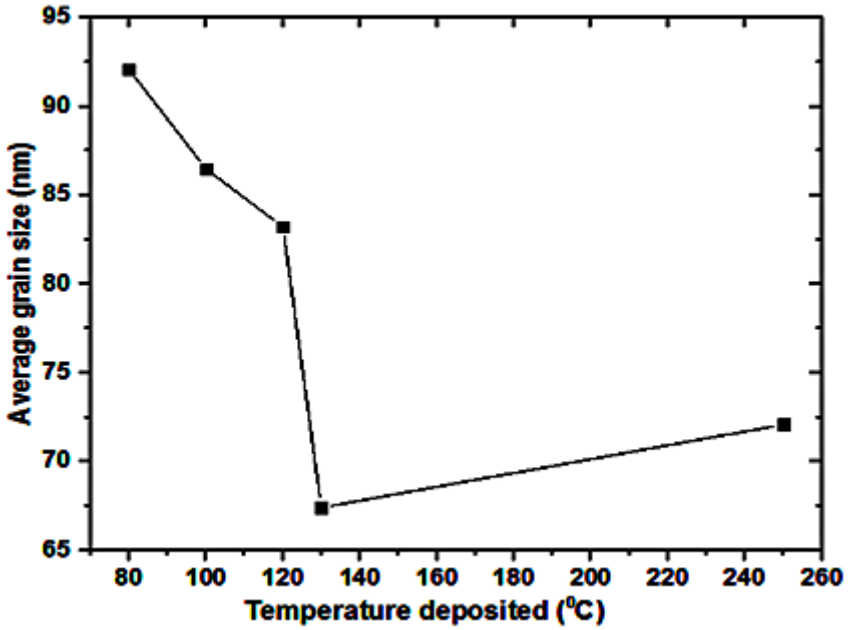


Figure IV-22:The average grains size as a function of the deposition temperature.

The fabrication methodology of the nc-ZnO TFT is detailed in [132]. The measured dependence on deposition temperature of the transfer characteristics will be compared to simulation later.

The relationship between the average grain size of a material and the sedimentation temperature can vary depending on several factors, including the material used, the method of sedimentation, and the specific conditions of the sedimentation process. However, in general, in this study, increasing the deposition temperature leads to a decrease in the average grain size of the material. Assuming that the information provided refers to the average grain size of a particular material, such as a thin layer of semiconductor or oxide, we can conclude that the average grain size decreases as the deposition temperature increases from 80 to 130°C and then slowly increases up to 250°C. Specifically, the average grain size appears to decrease from 86.5 nm at 80 °C to 72.06 nm at 130 °C and then gradually increase to 67.44 nm at 250 °C.

It should be noted that other factors, such as the precipitation method, precursor concentration, and substrate material, can also influence the grain size of the material. Therefore, the exact relationship between deposit temperature and grain size can vary depending on the specific experimental conditions used.

IV.4.2 Computational modelling of the nc-ZnO thin film transistor

A three-dimensional cross section of the nc-ZnO TFT structure used in this work is shown in Fig.3. The channel is 10 nm thick nc-ZnO, the substrate is a heavily doped p-type poly-silicon which also acts as a gate, the gate insulator is a 20 nm thick Al_2O_3 layer, the drain and source ohmic contacts are 2.5 µm long aluminum (Al). The separation between the source and drain is 40 µm. The width of the TFT is 50 µm.

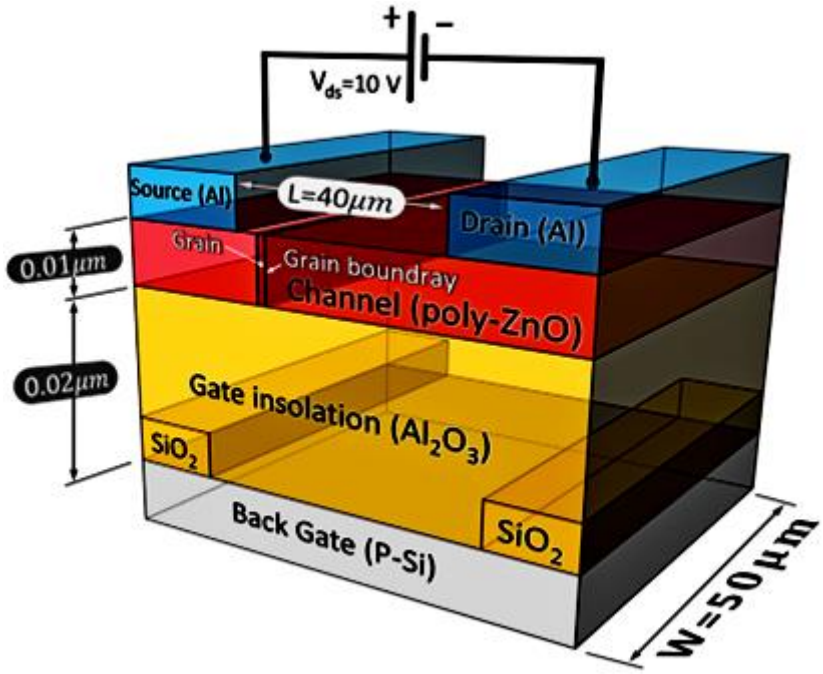


Figure IV-23:A three-dimensional view of the nc-ZnO TFT simulated in this work.

In order to simulate the electrical behavior of the device, we introduce equally spaced granules with the same thickness as the zinc oxide (ZnO) layer. These granules represent the nanocrystalline structure of the nc-ZnO layer. The simulations are performed using SILVACO, a simulation tool specifically designed for analyzing the electrical performance of thin-film transistor (TFT) displays. SILVACO enables us to predict key electrical characteristics of the TFT, including the drain current, subthreshold swing, and on/off current ratio, under various operating conditions. Through careful analysis of the simulation results obtained from SILVACO, we can optimize important device parameters such as the channel length and grain

size. This optimization process aims to enhance the overall performance of the nc-ZnO TFT, ultimately leading to the development of high-performance TFT displays suitable for a wide range of applications.

The parameters used in the TFT simulation are extracted by fitting the simulated and measured I-V characteristics except the electron affinity and dielectric constant at different temperatures ranging from 80 to 250 °C. The parameters at 100°C are presented in

Table IV-4.The nano-crystalline ZnO thin film transistor is defined by introducing equally spaced grains parallel to the ZnO film thickness and perpendicular to the direction of carrier propagation from source to drain.

Table IV-4:The parameters of nc-ZnO TFT used in this work for 100°C.

Parameter	**Grain**	**Grain boundary**
Electron affinity (known)	4.29 eV	4.29 eV
Dielectric constant (known)	8.12	8.12
Electron mobility	30 $cm^2/V.s$	0.5 $cm^2/V.s$
Hole mobility	1.5 $cm^2/V.s$	0.1 $cm^2/V.s$
Effective conduction band states	1.5 10^{19} cm^{-3}	2.5 10^{18} cm^{-3}
Effective valence band states	1.5 10^{21} cm^{-3}	1.5 10^{20} cm^{-3}
Energy gap at 300K	3.4 eV	3.4 eV
Density of acceptor-like tail states	1.0 10^{20} $cm^{-3}.eV^{-1}$	1.05 10^{21} $cm^{-3}.eV^{-1}$
Density of donor-like tail states	1.0 10^{19} $cm^{-3}.eV^{-1}$	1.0 10^{17} $cm^{-3}.eV^{-1}$
Capture cross section of electron and hole	4.0 10^{-15} cm^2	4.0 10^{-15} cm^2
states Characteristic decay energy	0.13 eV	0.11 eV
acceptor-like tail states		

Characteristic decay energy donor-like tail states	0.1 eV	0.08 eV
Total density of acceptor-like Gaussian states	1.0 10^{19} $cm^{-3}.eV^{-1}$	1.0 10^{18} $cm^{-3}.eV^{-1}$
Total density of donor-like Gaussian states	1.0 10^{19} $cm^{-3}.eV^{-1}$	1.0 10^{17} $cm^{-3}.eV^{-1}$
Peak position of the acceptor-like Gaussian states	0.2 eV	0.19 eV
Peak position of the donor-like Gaussian states	0.4 eV	0.3 eV
characteristic decay energy donor and acceptor-like Gaussian states	0.15 eV	0.15 eV

Comparison between experimental [132] and simulated transfer characteristics of nc-ZnO thin-film transistors in the saturation region (V_{DS} = 10 V) are shown in Figure IV-24 on logarithmic.

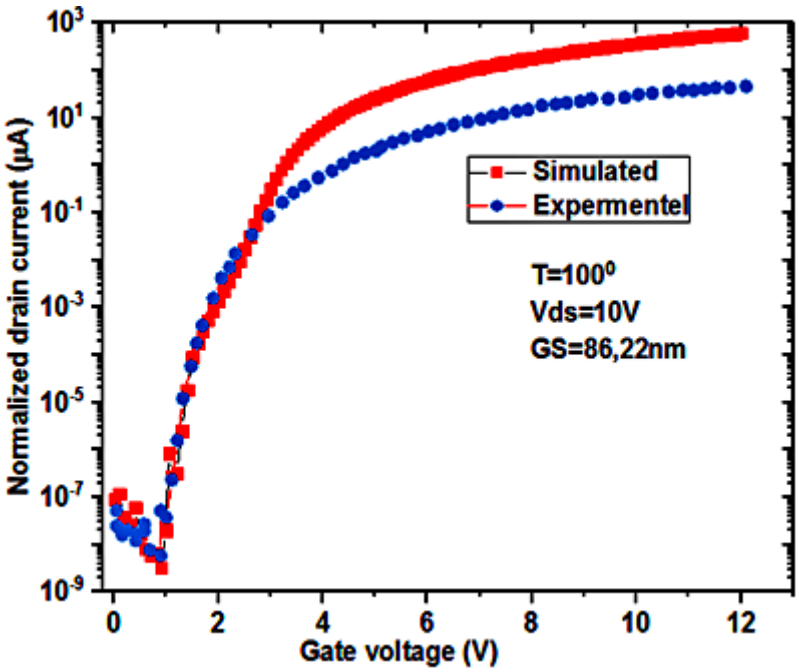


Figure IV-24:Experimental and simulated transfer characteristics $I_D = f(V_{DS})$ of the TFT for temperature 100℃.

Figure IV-24 experimental and simulated normalized transfer characteristics of nc-ZnO thin-film transistors at 100℃ . The inset is a linear representation of the same curve.

Comparison of experimental and simulated transfer characteristics of nc-ZnO thin film transistors in the saturation region (V_{DS} = 10 V) and grain size (86 .22 nm) involves plotting the drain current (I_D) as a function of the gate voltage (V_{GS}) of a constant voltage drain source (V_{DS}) 10 volts. The transfer characteristics show how the current flowing through the transistor changes as a function of the gate voltage, which is used to control the flow of current in the device.

In this case, the comparison is made for a temperature of 100 °C. The experimental transfer characteristics are obtained by measuring the drain current for different gate voltages while keeping the drain-source voltage constant at 10 V. On the other hand, the simulated transport characteristics are obtained by using a mathematical model of the device and solving equations to predict the behavior of the device under different conditions. In our case, we used the SILVACO program.

By comparing the experimental and simulated transport characteristics, the accuracy of the model used to simulate the device can be evaluated. Our experimental and simulated transport characteristics were closely matched, this indicates that the model is accurate and can be used to predict device behavior under different conditions. But if there are significant differences between the experimental and simulated transport characteristics, this indicates that the model needs to be improved or that there are other factors affecting the performance of the device that were not considered in the model.

For simulated, the TFTs must be searching for parameters of nc-ZnO for each temperature 80 to 250℃ as Table IV-4.

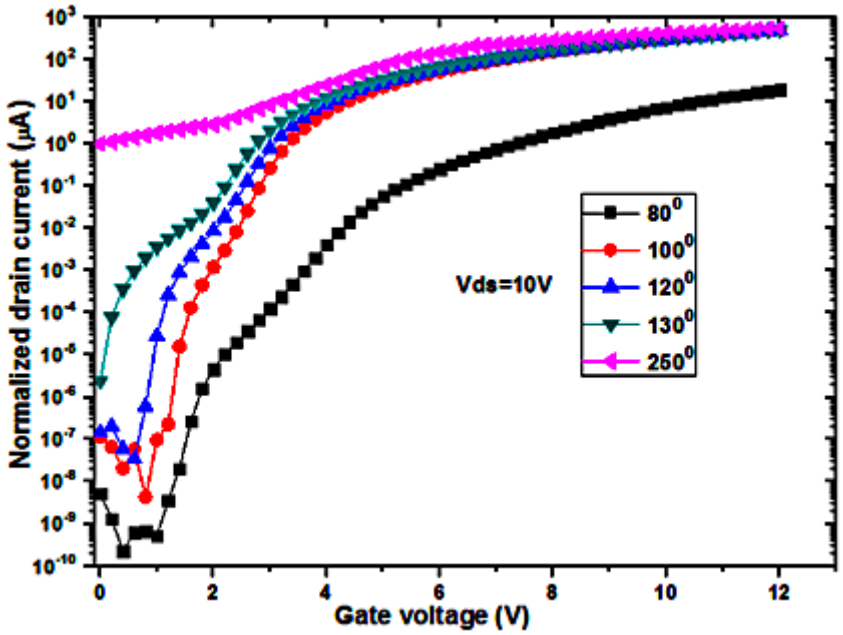


Figure IV-25:The simulated normalized transfer characteristics $I_D = f(V_{GS})$ of the TFTs (ZnO/Al_2O_3) for different growth temperatures ranging from 80 to 250℃.

The simulated $I_D = f(V_{GS})$ standardized transport characteristics of (ZnO/Al_2O_3) TFTs were obtained for different growth temperatures ranging from 80 to 250 °C using SILVACO simulation software. To achieve these results, simulations were run separately for each temperature, and the corresponding values of the TFT parameters were set to correspond with the experimental results.

Simulated curves show the variation of drain current (I_D) by gate voltage (V_{GS}) for each growth temperature. From the simulation results, it can be seen that the performance of the device improves with the increase of the growth temperature. This behavior can be attributed to changes in the crystal structure and defects that occur with increasing growth temperature. At lower growth temperatures (80-130 °C), the devices show reduced performance, with low drain current and a high subthreshold slope. As the growth temperature increases, the performance of the devices improves, with higher SS and lower threshold slope. The devices show the highest performance at around 200 °C as per the experimental results[132] .

The simulation results showed a good agreement with the experimental results, indicating the effectiveness of the SILVACO simulation software in predicting the performance of TFTs (ZnO/Al_2O_3) for different growth temperatures.

IV.4.3 Applied the temperature at nc-ZnO TFT

The applied temperature of the nc-ZnO TFT is simulated for temperatures ranging from 80 to 250℃ (high temperature), With selectable nc-ZnO TFT parameters for 80° growth. The transfer characteristics, the drain current versus gate voltage. In this case, a detailed numerical simulation is carried out to elucidate the experimental behavior of the temperature dependent characteristics current-voltage (I-V) characteristics of the nanocrystalline zinc oxide thin film transistor (nc-ZnO TFT). The temperature dependence of the TFT parameters (threshold voltage and the sub-threshold) was also clarified.

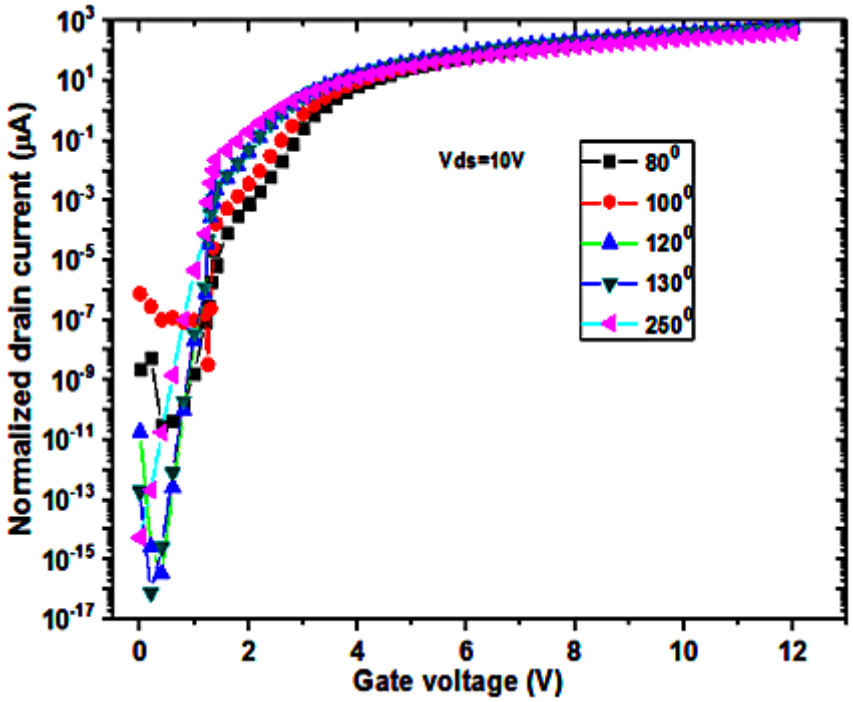


Figure IV-26:The simulated normalized transfer characteristics $I_D = f(V_{GS})$ of the TFTs for applied different temperatures ranging from 80 to 250℃.

Temperature is an important parameter in the operation of nano TFTs. The temperature affects the mobility of charge carriers, the threshold voltage, and the subthreshold swing of the device. As the temperature increases, the mobility of the charge carriers in the nc-ZnO TFT channel increases, which leads to an increase in the drain current of the device. However, if the temperature increases too much, the threshold voltage of the device may shift, leading to a change in the turn-on behavior of the device.

In addition, high-temperature operation can also cause reliability issues in the TFTs. For example, thermal stress can lead to material degradation and the formation of defects in the TFT

structure, which can reduce the lifetime and stability of the device. We see the difference between the temperature of the deposition (Figure IV-25) and the temperature applied to the channel or the semiconductor. We can calculate the activation energy of a transistor (see effect temperature).

IV.4.4 Extract threshold and sub-threshold swing at growth and applied temperature for nc-ZnO TFTs

The voltage threshold and subthreshold of ZnO TFT can be affected by various factors, including material properties, device structure, and operating conditions. In the case of nc-ZnO TFTs, the threshold voltage and sub-threshold swing can be affected by the grain size and grain boundary properties of the nc-ZnO layer, as well as the gate dielectric thickness, channel length and applied bias. Vth and SS can be experimentally extracted by measuring the drain current as a function of the gate-source voltage and fitting the data to an appropriate model.

Threshold voltage and SS can also be simulated using computational tools, such as TCAD or SPICE, by taking into account material properties, device structure and TFT operating conditions. These simulations can provide insight into the influence of various parameters on the threshold voltage, such as grain size, gate insulator thickness, or temperature. Based on previous research, it has been shown that the threshold voltage and SS of nc ZnO TFTs can be affected by the growth and applied temperature.

For a comparison of the threshold voltage and SS as a function of growth temperature applied for nc ZnO TFTs, experimental measurements and simulations have to be performed. Experimental measurements can include fabricating nc ZnO TFTs with different growth temperatures and measuring their threshold voltages under different bias conditions. The simulation will include modeling of the device structure and material properties of the TFT and simulating its electrical behavior as a function of the growth and applied temperature.

By comparing the experimental and simulation results, it will be possible to identify the main factors affecting the threshold voltage and SS of nc ZnO TFTs as a function of growth and applied temperature, and optimize the device parameters to improve the overall performance of the TFT.

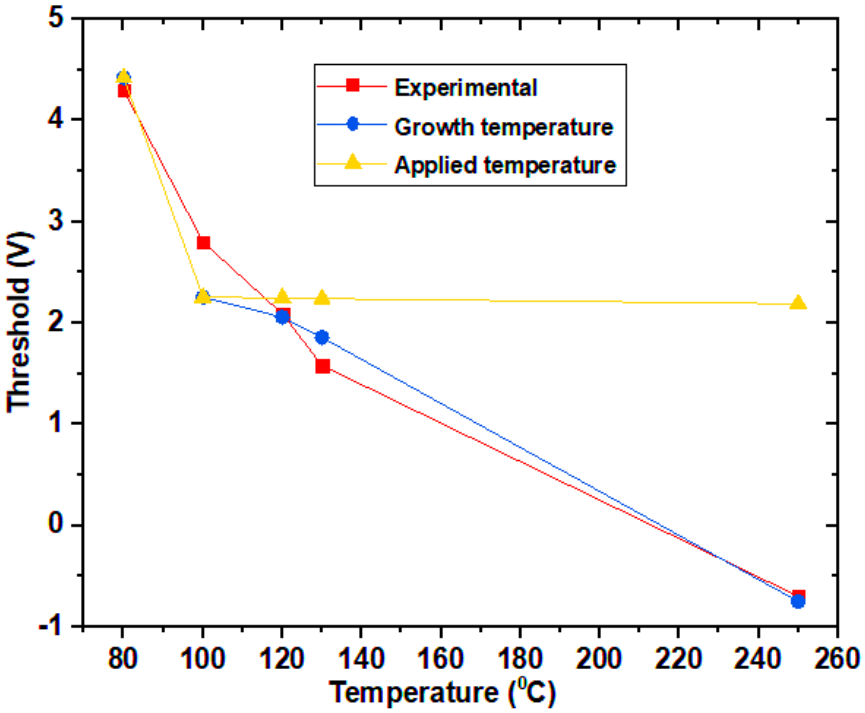


Figure IV-27:Comparison of threshold voltage experimentally by simulation extracted as function of temperature the growth and applied.

Based on the comparison of the experimental and simulation results for the threshold voltage of nc-ZnO TFTs, it was found that the higher the growth temperature or the applied temperature, the lower the threshold voltage. The decrease in the threshold voltage with increasing growth temperature is more significant and can reach up to -1 V, which corresponds to the modeled curve. On the other hand, for the applied temperature, the threshold voltage curve drops quickly from 80 to 100 degrees Celsius to 2.25 V and then stabilizes, irrespective of the temperature changes. These findings suggest that the growth and applied temperatures have a significant impact on the threshold voltage of nc-ZnO TFTs, and careful optimization of these parameters can improve the performance of the TFT.

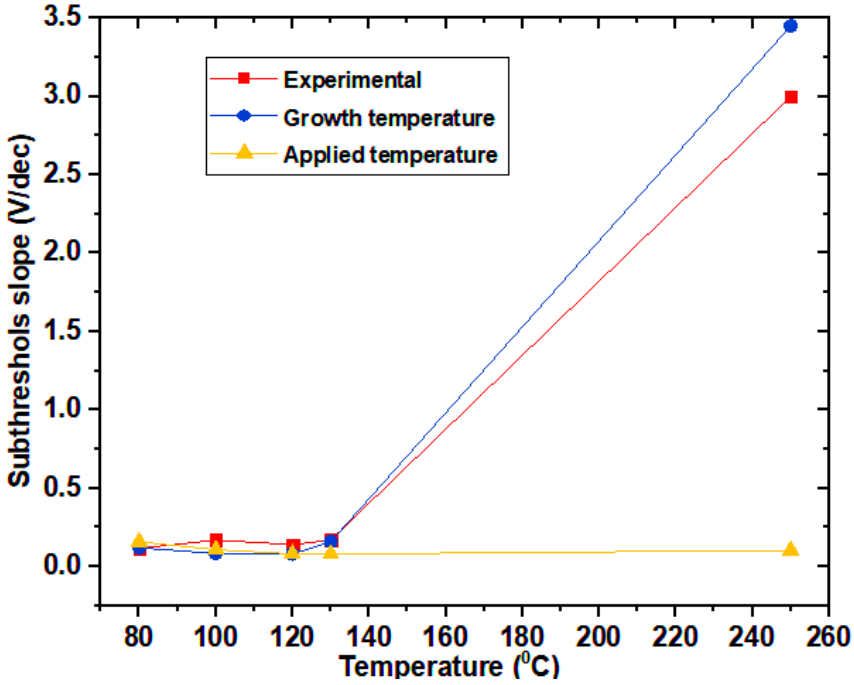


Figure IV-28:Comparison of sub-threshold slop experimentally by simulation extracted as function of temperature the growth and applied.

Sub-threshold swing is an important parameter that determines the switching performance of a transistor. Lower subthreshold swing corresponds to better conversion performance. In this case, the experimental and simulated sub-threshold swing values of nc-ZnO TFTs grown at different temperatures ranging from 80 to 250 °C were compared.

The results show that the sub-threshold swing was held at 0.1 V/dec for growth temperatures up to 130 °C. After this temperature, the sub-threshold started to increase gradually with increasing growth temperature and eventually reached 3.44 V/dec at 250 °C and remained constant with respect to the applied temperature. Sub-threshold swing goes up. As the growth temperature increases, as a result the ZnO grains in the film are small and well dispersed, which leads to a greater number of grain boundaries and defects that act as traps for charge carriers, resulting in a higher subs ratio.

The simulation results were consistent with the experimental results, indicating that the simulation model was able to accurately capture the basic physics of device operation. These results provide important insights into the growth temperature dependence of the sub-threshold in nc-ZnO TFTs, which can be useful for optimizing growth conditions to improve device performance.

On the other hand, we observe that the value of the Vth and SS properties of the

simulation is close to the experimental at low temperatures (<130℃ ,400K) and away at higher temperatures (>130℃ ,400K). This is proven in the previous search (effect temperature). So we conclude that the effect of temperature applied to the pc-TFT has the same effect on the nc-TFT with respect to Vth and SS.

IV.4.5 Internal effects of growth temperature on nc-ZnO TFT

In ZnO TFTs, the electric field, voltage, and free electron concentration in the channel play a critical role in determining the device's performance. The electric field is the force that acts on a charged particle in an electric field and determines the particle's movement in the channel. The voltage applied to the gate electrode controls the electric field and modifies the free electron concentration in the channel, which directly affects the device's performance. The free electron concentration determines the electrical conductivity of the channel, and hence the current flowing through the device. Therefore, understanding the relationship between the electric field, voltage, and free electron concentration in the ZnO TFT channel is essential for optimizing the device's performance. In this context, extensive research has been conducted to investigate the underlying physics and improve the performance of ZnO TFTs.

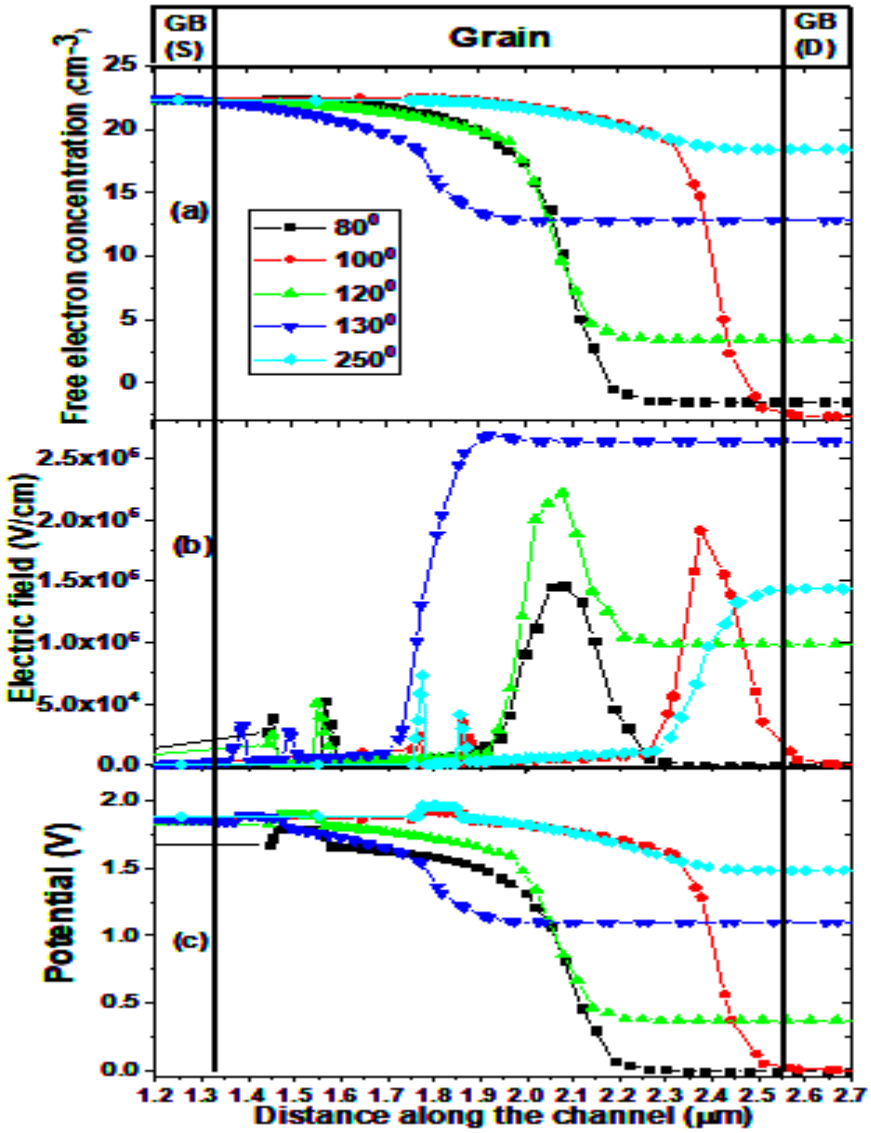


Figure IV-29:Cross section of potential (a), electric field (b) and free electron concentration (c) the grain layer for Nano-ZnO TFTs with temperature deposited at T= 80, 100, 120, 130 and 250℃.

In nc-ZnO TFT channel, the potential (V) plays a crucial role in determining the conductivity and current flow through the channel. The channel acts as a conductor when a certain threshold voltage is applied to the gate, which creates a channel between the source and drain. The potential difference between the gate and channel controls the amount of current flow through the channel, which is essential for proper device operation. If the potential is too low, the channel cannot conduct sufficient current, and the device will not function correctly. On the other hand, if the potential is too high, excessive current may flow through the channel, causing the device to overheat and malfunction. Therefore, controlling the potential is critical.

In nc-ZnO TFT channel, the electric field plays a significant role in determining the flow of charge carriers through the channel. The electric field in the channel is directly proportional to the potential difference between the source and drain electrodes. The applied gate voltage modulates the electric field, which controls the channel's conductivity and the current flow through it. When a voltage is applied to the gate, it induces a charge distribution in the channel region, creating an electric field that drives the charge carriers from the source to the drain. The strength of the electric field determines the mobility of the charge carriers, which in turn affects the conductivity of the channel. A higher electric field results in a higher current density through the channel and vice versa. In addition to determining the current flow, the electric field also affects the performance and stability of the device. Excessive electric fields can cause charge carrier trapping and mobility degradation, leading to device failure. Therefore, it is essential to carefully control the electric field in the channel region to ensure optimal device performance and reliability.

In nc-ZnO TFT channel, the free electron concentration is an important parameter that affects its electrical performance. It is directly related to the conductivity of the channel and is therefore critical to the operation of the device. The free electron concentration is influenced by the density of states in the conduction band of the ZnO material, as well as by the doping concentration and the temperature. In general, an increase in the free electron concentration results in a higher conductivity and a lower resistance in the channel, which can lead to better device performance. However, excessively high free electron concentrations can also lead to undesirable effects such as increased leakage current and instability of the device. Therefore, controlling the free electron concentration is an important aspect of optimizing the performance of ZnO TFTs. The growth temperature during the fabrication process can also affect the free electron concentration in the ZnO material. As the growth temperature increases, the density of oxygen vacancies in the ZnO material decreases, which can lead to a reduction in the free electron concentration. On the other hand, a higher growth temperature can also lead to larger grain sizes and fewer grain boundaries, which can increase the mobility of free electrons in the channel and therefore lead to a higher free electron concentration. Therefore, finding the optimal growth temperature to achieve the desired free electron concentration is a crucial step in the fabrication of high-performance ZnO TFTs.

IV.4.6 Simulation thin film transistors-based Si/Al_2O_3

The development of high-performance TFTs with low cost, high stability, and excellent electrical properties has been the subject of intense research in recent years. Two promising materials for TFT applications are silicon (Si) and zinc oxide (ZnO) due to their unique properties. However, to improve the performance of TFTs, it is necessary to understand the effect of different parameters on their electrical properties, such as temperature. In this context, simulation of TFTs is a powerful tool to investigate device behavior under different conditions. In this study, we simulate Si/Al2O3 based thin-film transistors with the same dimensions as nc-ZnO/Al_2O_3, and compare the normalized $I_D = f(V_{GS})$ transfer characteristics of the two devices for different applied temperatures ranging from 80 to 250 °C. This comparison will provide insight into the effect of temperature on the electrical properties of TFT displays, which can help improve their performance for different applications.

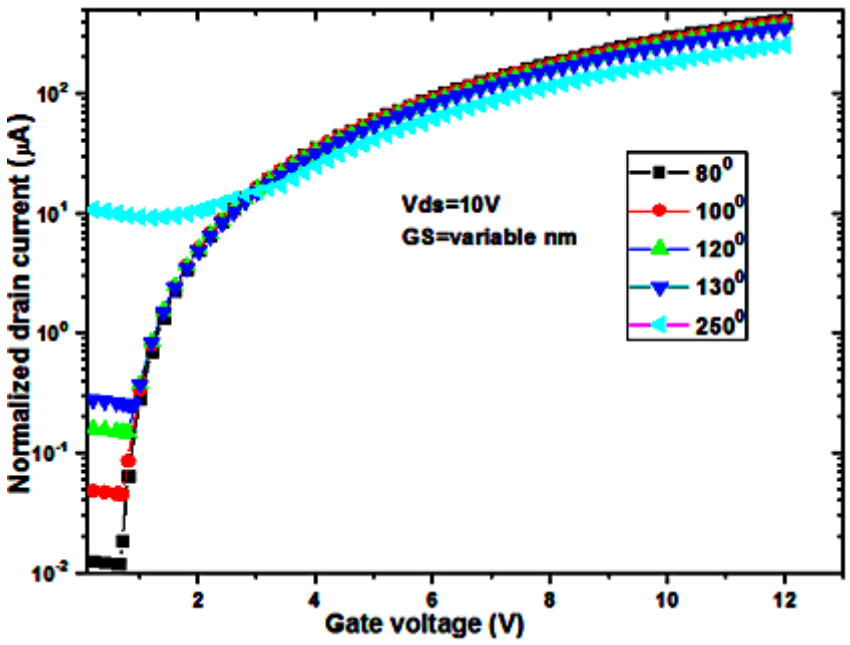


Figure IV-30:The simulated normalized transfer characteristics $I_D = f(V_{GS})$ of the TFT (Si/Al_2O_3) for different temperatures ranging from 80 to 250℃.

IV.4.7 The effect of design grain

In the design of nanocrystalline zinc oxide thin-film transistors (nc-ZnO TFTs), the grain structure plays a crucial role in determining the electrical performance of the device. In particular, the two-dimensional grain design, which includes both length and width, can significantly impact the threshold voltage, leakage current, and subthreshold swing of the TFT. This is because each grain in the TFT can have a different electrical behavior, depending on

factors such as size, orientation, and crystallographic defects. Additionally, the presence of grain boundaries between adjacent grains can also affect the device performance. Therefore, it is essential to study the impact of the grain design on the electrical properties of nc-ZnO TFTs to optimize their performance and reliability. In this context, the two-dimensional grain model has been extensively used to investigate the behavior of nc-ZnO TFTs and provide insights into their electrical characteristics.

IV.4.7.1 The effect of grain length on nc-ZnO TFTs

One of the key parameters that can affect the performance of nc-ZnO TFTs is the grain length. In these TFTs, the grains have a two-dimensional (length and width) design in a single-grain model, and each grain has a grain boundary that can significantly affect the electrical properties of the TFT. Therefore, understanding the effect of grain length on the performance of nc-ZnO TFTs is essential for their optimal design and performance. In this context, this topic will explore the impact of grain length on the threshold leakage current and subthreshold swing of nc-ZnO TFTs, providing insights into the design and optimization of these devices.

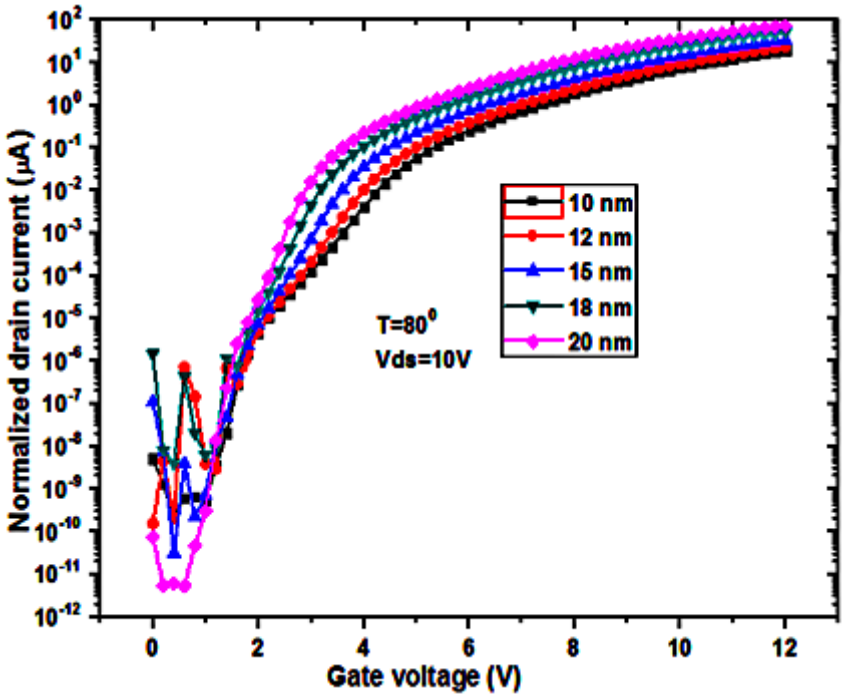


Figure IV-31:The simulated transfer characteristics $I_D = f(V_{GS})$ of the TFT for T=80℃ at length grain ranging from 10 to 20 nm.

The curve (a) shows the relationship between threshold voltage and grain length in nc ZnO TFT. It demonstrates a linear decrease in threshold voltage from 4.4 V to 3.6 V as the grain length increases from 0.01 to 0.02 micrometers. This relationship between the two variables

can be explained by the fact that longer grain length results in better connectivity and less scattering of electrons, leading to improved carrier transport properties. As a result, the threshold voltage decreases with an increase in grain length. This information can be used to optimize the performance of nc-ZnO TFTs by controlling the grain length during the manufacturing process.

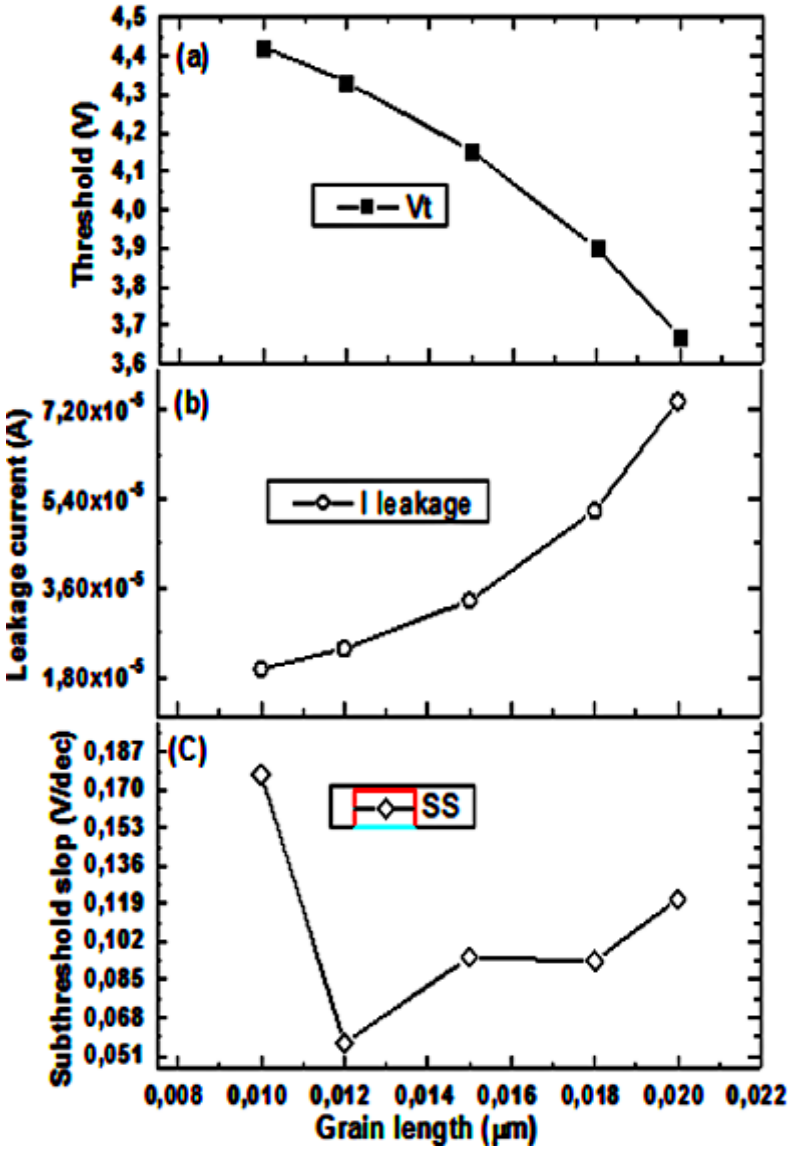


Figure IV-32:Curve (a) Threshold (b) Leakage current (c) Subthreshold slop versus grain length.

The performance of nano ZnO TFTs is affected by the grain size and grain boundaries in the channel region. As discussed earlier, the threshold voltage of the TFTs decreases linearly with increasing grain length. However, another important factor that affects the performance of the TFTs is the leakage current. It has been observed that the leakage current in the TFTs increases linearly with increasing grain length. This phenomenon can be explained by

considering the effect of grain boundaries on the transport of carriers in the channel region.

In n-c ZnO TFT, the grain boundaries act as potential barriers that can trap the charge carriers (electrons or holes) and reduce their mobility. As the grain size increases, the number of grain boundaries in the channel region also increases, leading to an increase in the number of potential barriers. This, in turn, increases the probability of trapping of the charge carriers and reduces their mobility, leading to an increase in the leakage current. The leakage current in a n-c ZnO TFT can be modeled using the Shockley-Read-Hall (SRH) recombination mechanism. According to this mechanism, the leakage current is proportional to the concentration of traps in the channel region, which is dependent on the grain size and the density of grain boundaries. As the grain size increases, the number of grain boundaries in the channel region increases, leading to an increase in the density of traps and an increase in the leakage current.

The effect of grain boundaries on the leakage current can be further explained by considering the relationship between the carrier mobility and the grain size. As the grain size decreases, the carrier mobility increases due to the reduction in the number of potential barriers. This leads to a decrease in the leakage current. On the other hand, as the grain size increases, the number of potential barriers and the density of traps increase, leading to a decrease in the carrier mobility and an increase in the leakage current. Therefore, it is important to optimize the grain size and the density of grain boundaries in the channel region to achieve a balance between the threshold voltage and the leakage current in n-c ZnO TFTs. A trade-off between these two parameters is necessary to achieve high-performance TFTs. A smaller grain size can lead to a decrease in the threshold voltage but an increase in the leakage current, while a larger grain size can lead to a decrease in the leakage current but an increase in the threshold voltage.

The leakage current in nano ZnO TFTs increases linearly with increasing grain length due to the increased density of potential barriers and traps in the channel region. This can be attributed to the effect of grain boundaries on the transport of carriers in the channel region. To achieve high-performance TFTs, a balance between the threshold voltage and the leakage current needs to be achieved by optimizing the grain size and density of grain boundaries in the channel region.

The curve (c) shows the relationship between the subthreshold slope and the grain length in nano ZnO TFT. It can be seen that the subthreshold slope decreases from 0.187 V/dec at 0.01

µm to 0.051 V/dec with a fast slope and then slowly rises to 0.102 V/dec at 0.02 µm.

Therefore, in the case of curve (c), it can be observed that the subthreshold slope decreases rapidly at smaller grain lengths due to the increasing influence of the grain boundary trap states on the channel, which leads to a decrease in the carrier mobility. However, at larger grain lengths, the effect of the grain boundary on the subthreshold slope becomes less pronounced, and the slope increases slowly. On the other hand, the leakage current increases linearly with grain length, indicating that longer grain boundaries result in more defects and trap states, which in turn increase the leakage current.

In conclusion, the effect of grain size on the performance of nc- ZnO TFTs is a complex issue, and different trends can be observed for different performance parameters. While increasing grain size can lead to a decrease in threshold voltage, it can also lead to an increase in leakage current. Therefore, the design of nc-ZnO TFTs should take into account the trade-off between the desired performance parameters and the grain size, as well as other factors that can affect the performance of the device.

IV.4.7.2 The effect of grain width on TFTs

In our study, we investigated the effect of grain width on the electrical properties of nc-ZnO TFTs. Changing the grain width from 50 µm to 130 µm resulted in an increase in leakage current from 2 10^5 A to 5 .10^5 A and an increase in out-of-case current by three orders of magnitude. This is attributed to the increased dispersion of the carriers due to the grain boundaries.

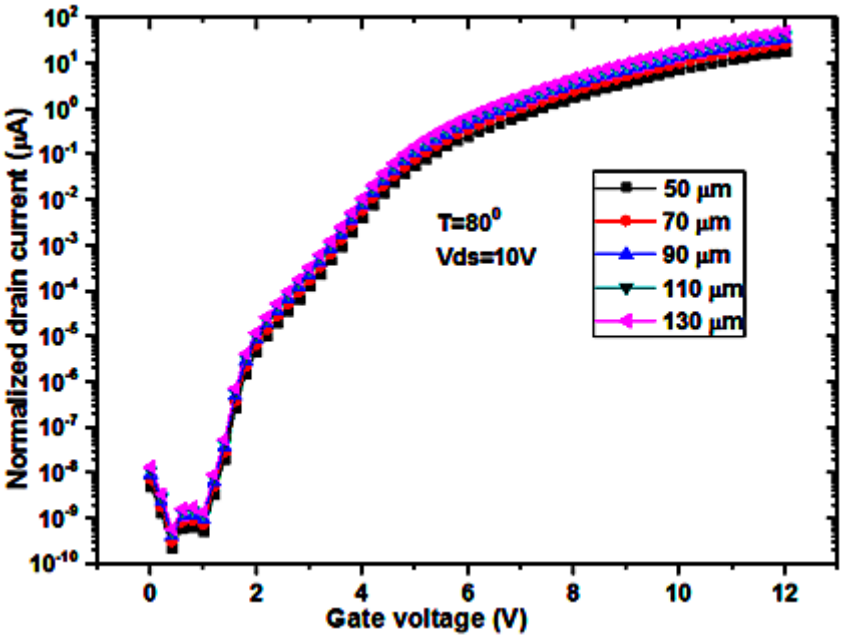


Figure IV-33:The simulated transfer characteristics $I_D = f(V_{GS})$ of the TFT for T=80°C at width grain ranging from 50 to 130 µm.

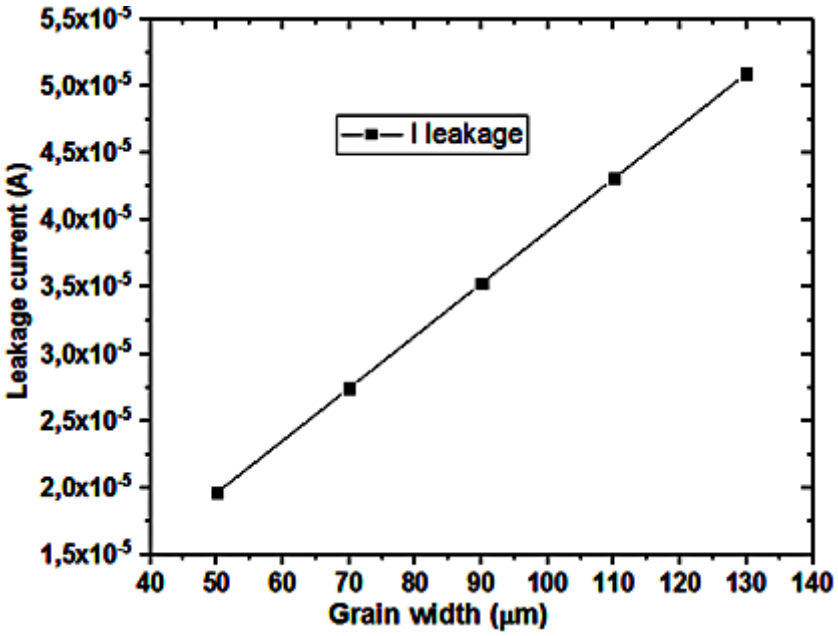


Figure IV-34:Leakage current function grain width.

In nc-ZnO TFT, the width of the grain can have an impact on various electrical parameters, including the threshold voltage, subthreshold swing, and leakage current. However, research has shown that while the threshold voltage and subthreshold swing remain relatively constant with increasing grain width, the leakage current tends to increase.

This phenomenon can be attributed to the fact that the threshold voltage and

subthreshold swing are determined by the density of states in the channel, which does not change significantly with grain width. On the other hand, the leakage current is affected by the number of defects and impurities in the grain boundaries, which can increase with increasing grain width. Therefore, as the grain width increases, the number of grain boundaries also increases, leading to a higher probability of defects and impurities in the grain boundaries, resulting in increased leakage current.

In conclusion, as the grain size decreases, the surface area of the film increases, which can increase the number of defects and impurities at the grain boundaries. This can lead to increased electrical resistance and reduced carrier mobility, which can negatively impact the performance of the TFT. However, if the deposition temperature is carefully controlled, it is possible to produce TFT films with nanoscale grain sizes that have desirable properties. For example, at lower deposition temperatures, the grain size can be reduced while minimizing the number of defects at the grain boundaries. This can lead to increased carrier mobility and improved device performance.

On the other hand, higher deposition temperatures can result in larger grain sizes and reduced grain boundary density, which can also improve TFT performance. This is because larger grains can provide a more continuous and uniform conductive path for carriers to flow through, resulting in lower resistance and increased mobility. Therefore, the optimal deposition temperature for producing TFT films with desirable properties will depend on several factors, including the material being used and the specific application requirements.

IV.5 Fabrication of ZnO thin film transistors by PVD deposition method

IV.5.1 Fabrication of ZnO TFTs

A thin-film transistor (TFT) is a special kind of field-effect transistor made by depositing thin films of an active semiconductor layer as well as the dielectric layer and metallic contacts over a supporting (but non-conducting) substrate. As seen in Figure IV-35, the gate is insulated from the semiconductor film by a gate insulation film; while the drain and source directly contact the semiconductor film. A voltage applied at the gate controls the flow of electrons (resistance) from the source to the drain.

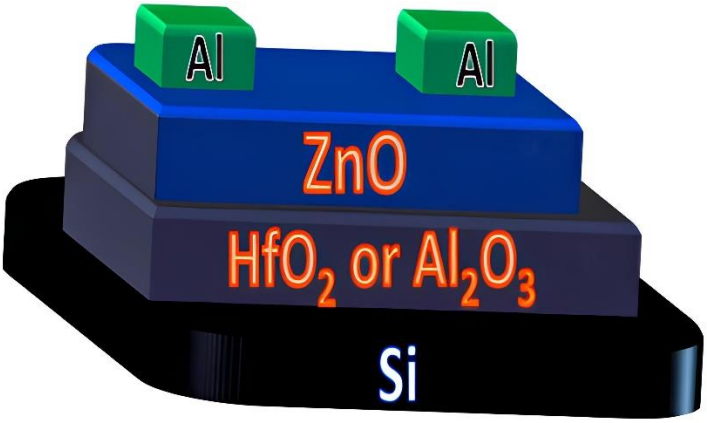


Figure IV-35:ZnO thin film transistors fabricated.

A diagram illustrating the structure of the bottom-gate-type zinc oxide thin-film transistors (TFTs) fabricated in this study is presented in Figure IV-36. The gate insulators consisted of 100 nm-thick layers of hafnium oxide (HfO_2) and aluminum oxide (Al_2O_3). The zinc oxide (ZnO) thin films were deposited onto the HfO_2 and Al_2O_3 gate insulators, while aluminum (Al) layers were deposited as the source and drain (S/D) electrodes using DC deposition and a shadow mask. The TFTs had a channel length of 1000 µm and a width of 30 µm. The electrical characterization of the TFTs was performed using a semiconductor parameter analyzer (Agilent 4156C). The TFT devices were fabricated on a silicon (Si) substrate, with the zinc oxide material serving as the channel layer.

The thin film deposition was carried out using a physical vapor deposition (PVD) method at a temperature of 100°C. The output characteristics of the TFT devices exhibited a decrease in drain current with an increase in drain-source voltage and gate-source voltage. This behavior indicated the presence of a self-heating effect, which could be attributed to an increase in donor-type point defects within the device structure. The electrical properties of the TFT device demonstrated an enhanced intrinsic channel mobility of 10 cm^2/Vs, a threshold voltage ranging from 12 to 14.7 V, a sub-threshold swing of 0.5 to 2 V/decade, and a significantly reduced off current on the order of 10^{-8} A.

IV.5.1.1 Cleaning the substrate

Before thin films deposition the substrate must be carefully cleaned to achieve better adherence and homogeny films. The cleaning steps used Al_2O_3/Si; HfO_2/Si substrate are presented below.

- Step 1 Soap cleaning: A liquid soap is used to remove oil, fingerprint from substrate.

- Step 2 Acetone cleaning: Acetone is used for removing any organic compound. The glass substrate is put in warm (less than 55°C) Acetone for 10 minutes. The glass substrate is placed in methanol for 2-5 minutes.

- Step 3 Cleaning by Isopropanol or isopropyl alcohol (IPA): The substrate is immersed in Isopropanol for 10 mins.

- Step 4 Deionized Water cleaning: The substrate is immersed in deionized water of 10 min.

Between each step we should put substrate in DI water for 1 mn and it is blow dried with nitrogen gas or air flow.

Each solution can be made on a heated bath or ultrasonic bath to improve the cleaning effect.

IV.5.1.2 Deposit of ZnO

ZnO thin films are deposited on Al_2O_3/Si, HfO_2/Si and glass substrates. Zinc oxide powder is used as a source of zinc vapor for zinc oxide deposition. Substrates inserted inside the deposition chamber which then evacuated using a combinational rotary and oil diffusion vacuum pumps to a base pressure of 1.10^{-5} mbar. The total pressure of the chamber during deposition is controlled at 3.10^{-3} mbar. Time od deposition is 10 S. the films annealed at 400°C for 2 h on air.

IV.5.1.3 Electrode deposition

After deposition of ZnO on Al_2O_3/Si, HfO_2/Si, a shadow mask is laid on top of the semiconductor. This mask is also used to define length and width of channel (L and W). Many methods can used to deposit the metallic contact. Thermal evaporation and DC sputtering are two methods widely used for deposited metallic contact. Figure IV-36 is an illustration to show

how shadow mask is used to define length and width of the metallic contact.

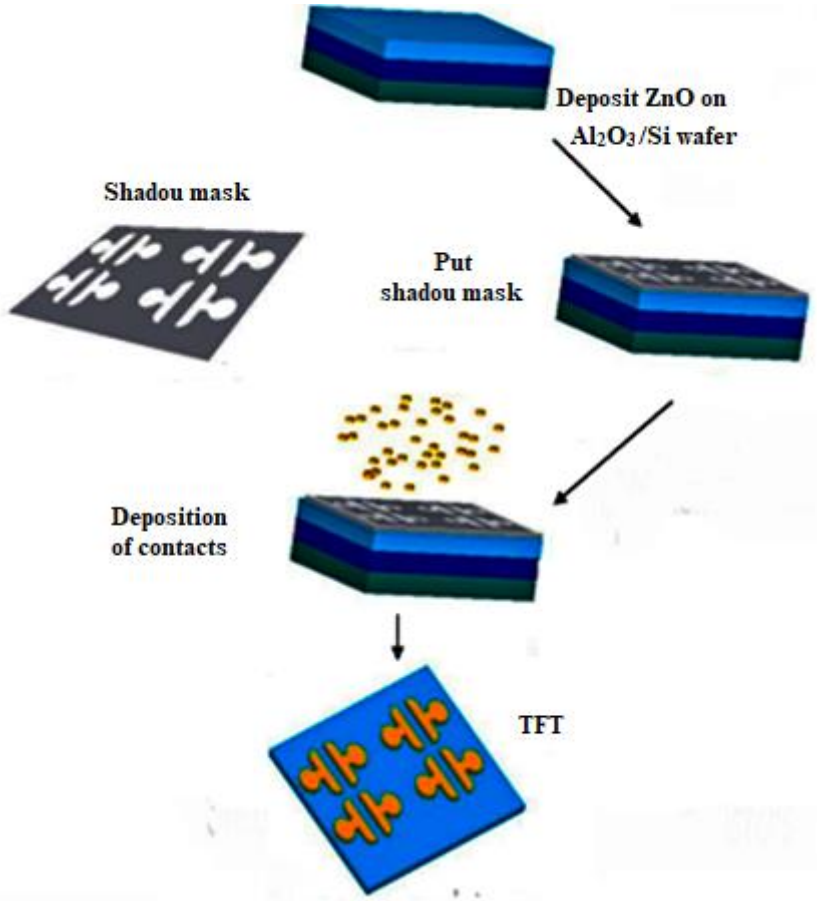


Figure IV-36:The illustration showing how shadow mask is used.

IV.5.2 Characterization and extract parameters of oxide zinc TFTs

The characterization of oxide zinc thin-film transistors (TFTs) typically involves both structural and electrical characterization. The structural characterization is used to determine the physical and chemical properties of the device layers, while the electrical characterization is used to extract the device parameters and performance metrics.

Structural characterization techniques include:

1. X-ray diffraction (XRD): This technique is used to determine the crystal structure and orientation of the ZnO layer, which affects the electrical and optical properties of the TFT.

2. Optical microscopy (OM): OM is used to measure the shape and surface dimensions of a TFT.

3. Scanning electron microscopy (SEM): SEM is used to determine the surface morphology and thickness of the various layers in the TFT structure.

Electrical characterization techniques include:

Various methods are used to evaluate how well Zinc Oxide Thin Film Transistors (ZnO TFTs) perform and how reliable they are. For instance, voltage (I V) testing measures the flow between the source and drain electrodes in relation to the voltage applied to the gate electrode. This helps in determining parameters like threshold voltage and mobility. Capacitance voltage (C V) testing assesses the properties of the gate dielectric, such as its constant and thickness, by observing changes in capacitance with gate voltage. Frequency response analysis looks at how ZnO TFTs behave at signal frequencies, providing insights into factors like gain and bandwidth. Bias stress testing involves monitoring changes in threshold voltage over time under bias conditions to assess device stability. Noise analysis helps extract information about carrier concentration, mobility and resistivity by studying the levels of device noise. By using these methods a thorough understanding of ZnO TFT performance.

IV.5.2.1 Structures characterization

Structural characterization is an essential aspect of understanding the performance of ZnO thin-film transistors (TFTs). Various techniques are employed to investigate the structural properties of these devices, including X-ray diffraction (XRD), optical microscopy (OM), and scanning electron microscopy (SEM). XRD is used to determine the crystallinity and orientation of the ZnO film, while OM and SEM provide valuable information on the morphology, grain size, and surface characteristics of the TFTs. By using these techniques, we can gain insight into the structural properties of ZnO TFTs and how they affect their electrical performance.

IV.5.2.1.1 X-ray diffraction (XRD)

The diffractograms obtained as well as the information that can be drawn from them are presented below. Indeed, and as already mentioned in chapter I, the diffractograms allow us to determine the reticular planes and the structure of the coating as well as the crystal lattice of the grains of the coating formed and this for the different experimental conditions considered. For this, the calculations are carried out using equations $D = \frac{0.94\lambda}{\Delta\beta_{hkl}.cos\theta_{hkl}}$ (I-3) and $\sigma = \left[2C_{13}.\frac{(C_{11}+C_{12}).C_{33}^{layer}}{C_{13}}\right]e_{zz}$ (I-4) and for each diffractogram analyzed, a result table is

drawn up. The X-ray diffraction analysis of the various deposits led to the following results:

XRD diagram (Figure IV-37) illustrates of sharp peak, the peak appeared at 2θ = 34.61 corresponds to the plane (002), Which reveal using ASTM database, the structure of ZnO (hexagonal (a = b, c, α = β = 90°, γ = 120°)).

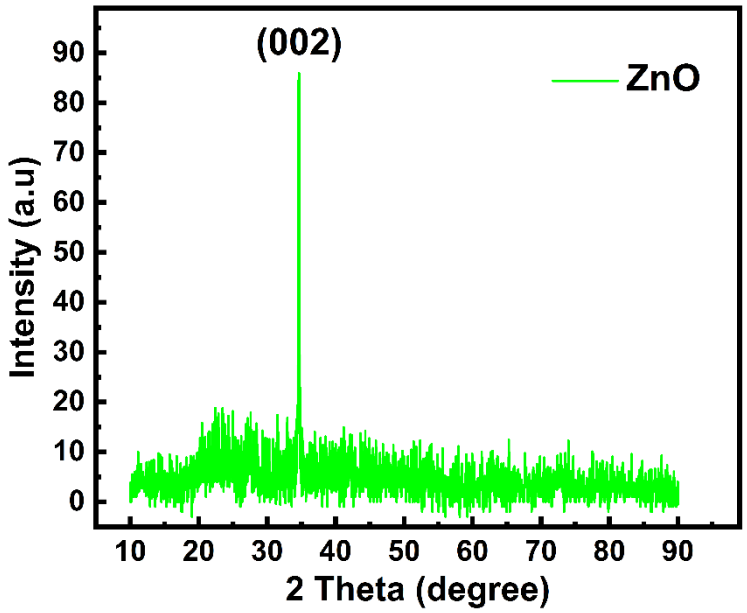


Figure IV-37:X-ray diffractogram analysis of our ZnO thin films.

Through the X-ray diffraction spectrum of our ZnO thin films, we can obtain the results shown in Table IV-5.

Table IV-5**:** The orientations of ZnO.

2θ (°)	$d_{(hkl)}$= nλ /2sinθ	N= $h^2 + k^2 + l^2$	(hkl)	intensity (u.a)
34,6194	2,5889	4	(002)	81.6753

Based on the X-ray diffraction (XRD) analysis of the ZnO channel for TFT, it can be concluded that the peak appeared at 2θ = 34.61 corresponds to the plane (002), which is indicative of the hexagonal structure of ZnO (a = b, c, α = β = 90°, γ = 120°) according to the ASTM database. This information can be useful for understanding the crystal structure of the ZnO channel and its impact on the performance of the TFT. Additionally, XRD analysis can provide valuable information about the quality of the ZnO thin film, such as its crystallinity and orientation. XRD is an important tool for the structural characterization of ZnO TFTs and can contribute to the optimization of their performance.

IV.5.2.1.2 Optical microscopy (OM)

Optical microscopy (OM) is a widely used technique in the structural characterization of ZnO thin-film transistors (TFTs). OM is a non-destructive imaging technique that provides high-resolution images of the sample surface. It is particularly useful for analyzing the microstructure and morphology of the ZnO TFTs, such as the grain size, grain boundary distribution, and surface roughness. By observing these features through OM, we can gain insights into the growth and fabrication processes of the ZnO TFTs, as well as their potential electrical performance. In this way, OM is an important tool for both fundamental research and practical applications of ZnO TFTs.

In the following figures, it is shown illustrated typical device structures that are adopted in the fabrication of ZnO TFTs. The TFT structure can be specified by the stacking order for the gate, oxide semiconductor, and source/drain electrodes. They can be classified more precisely into combinations of top/bottom gate and top/bottom contact (see chapter II). The top-gate structure was employed to fabricate devices with epitaxial semiconductor layers, for which it is difficult to form bottom electrodes.

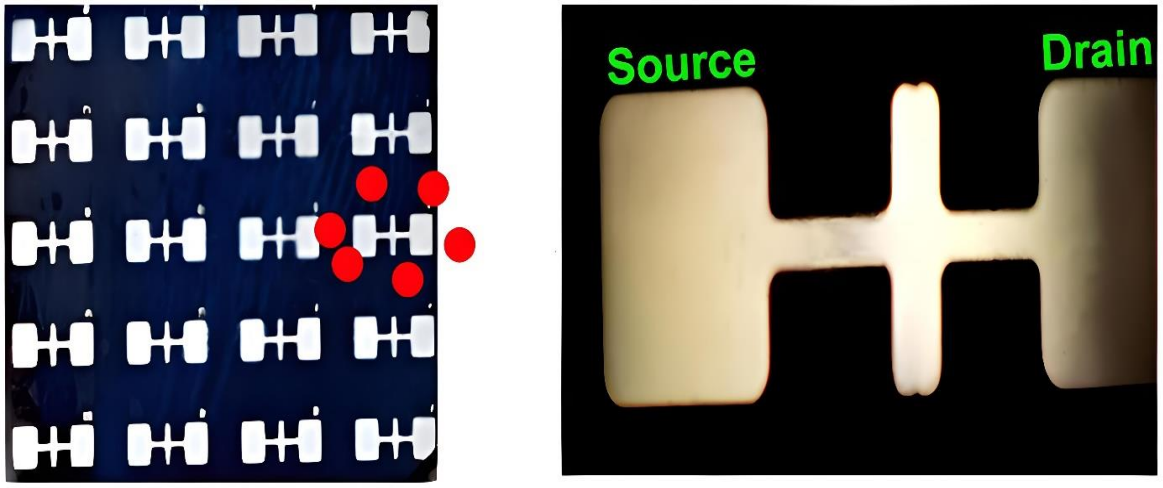


Figure IV-38: Image microscope of ZnO thin film transistors based (HfO_2/Si).

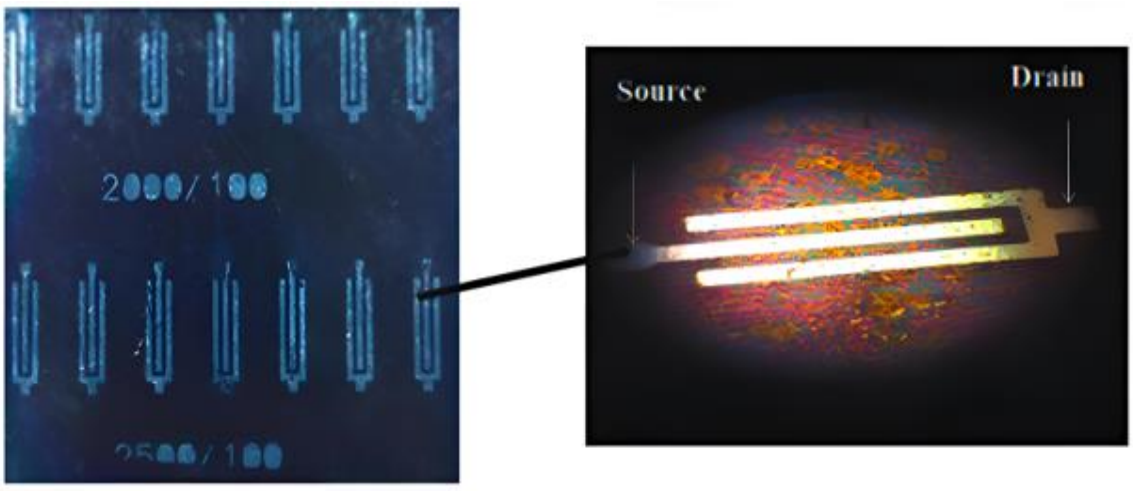


Figure IV-39: Image microscope of ZnO thin film transistors based (Al_2O_3/Si).

In conclusion, optical microscopy (OM) has been utilized to examine ZnO thin-film transistors (TFTs) based on different gate insulators, namely HfO_2/Si and $Al2O_3$/Si. The OM images provide valuable insights into the shape and dimensions of these devices, specifically the source-drain separation and width (W) between the two regions. By employing OM, the visual representation of the ZnO TFTs allows us to observe the physical structure and geometry of the devices. The images reveal the rectangular-shaped source and drain regions, with the channel region in between. The channel's width (W) is a critical parameter that influences the transistor's performance, including current flow and overall electrical characteristics. Moreover, OM images also illustrate the length (L) of the channel, representing the vertical distance between the source and drain electrodes. The channel length impacts the transistor's switching speed and current control, affecting its operational efficiency. The images obtained through OM also provide a clear view of the gate insulator layer, whether it is HfO_2/Si or $Al2O_3$/Si, positioned between the channel region and the gate electrode. This layer serves as an insulating barrier, controlling the flow of current through the channel.

IV.5.2.1.3 Scanning electron microscopy (SEM)

Structural characterization plays a crucial role in understanding the properties and performance of ZnO thin-film transistors (TFTs). One of the powerful techniques used for this purpose is scanning electron microscopy (SEM). SEM provides valuable insights into the morphology, surface topography, and structural details of the ZnO TFTs at high resolution.

In this introduction, we will explore the importance of SEM as a structural characterization technique for ZnO TFTs. By employing SEM, researchers can examine the

surface features, grain structure, and overall morphology of the thin-film transistors. SEM utilizes a focused beam of electrons to scan the surface of the sample, producing high-resolution images that reveal fine details at the nanoscale. One of the primary benefits of SEM is its ability to provide information about the surface roughness, grain size, and distribution within the ZnO thin films. The SEM images allow researchers to observe the crystal structure and grain boundaries, providing insights into the quality and crystallinity of the ZnO material. Additionally, SEM can help determine the presence of defects, impurities, or contaminants that may affect the device's performance. Furthermore, SEM can be used to measure critical dimensions such as the channel length, gate length, and gate oxide thickness in ZnO TFTs. These measurements are essential for characterizing the device's geometry and ensuring consistency in fabrication processes and simulation.

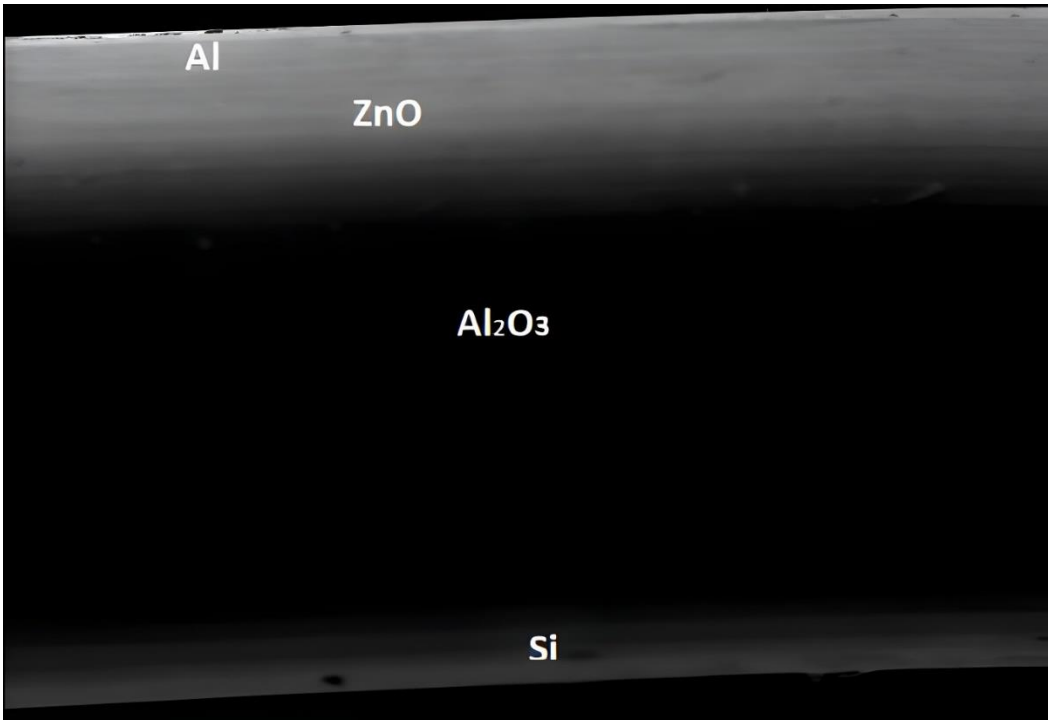


Figure IV-40: SEM image MAB of cross-section TFT (ZnO/Al_2O_3).

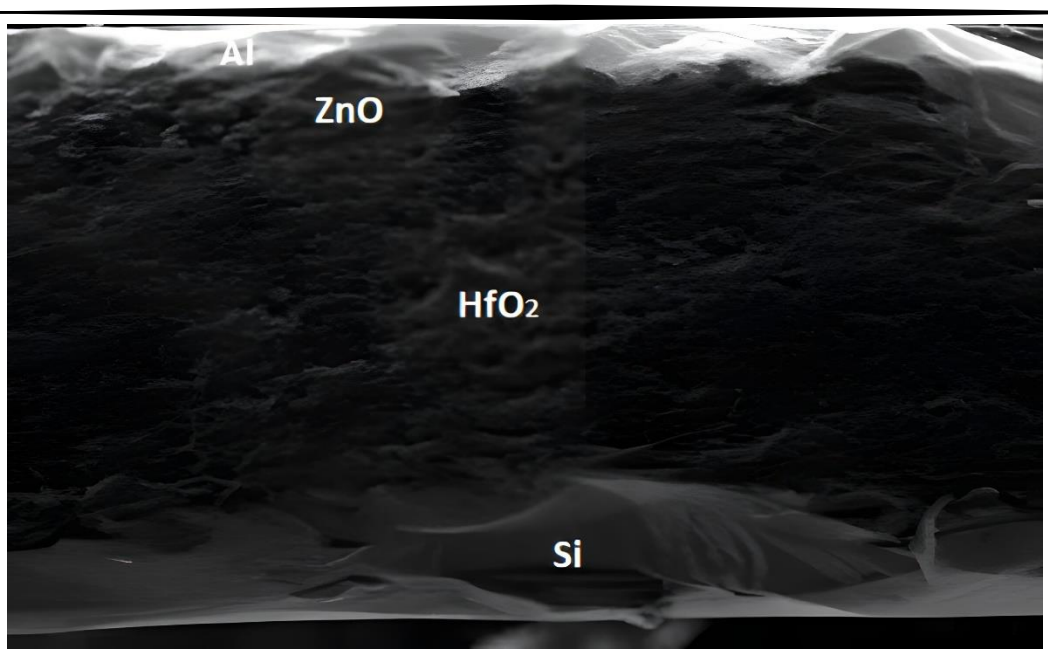


Figure IV-41:SEM image MAB of cross-section TFT (ZnO/HfO_2).

Scanning electron microscopy (SEM) is an invaluable technique for the structural characterization of ZnO thin-film transistors (TFTs) with different gate dielectric materials such as HfO_2/Si and $Al2O_3$/Si. The SEM images provide detailed information about the source and drain regions of the devices, as well as the differentiation between the layers of materials. By utilizing SEM, researchers can examine the dimensions and morphology of the ZnO TFTs, allowing for a comprehensive understanding of the device structure. The images obtained through SEM show distinct colors that correspond to different materials, enabling the differentiation between layers and providing insights into the layer thicknesses and uniformity. Moreover, SEM provides valuable information about the morphology of the materials used in the ZnO TFTs. It allows for the observation of surface features, including grain boundaries, surface roughness, and the overall texture of the films. These details are crucial for assessing the quality and crystallinity of the materials, which directly influence the device performance.

IV.5.2.2 Electrical characterization

The electrical characteristics which determine device performance are evaluated in terms of several parameters such as field effect mobility (μ_{FE}), threshold voltage (V_{th}), and subthreshold swing (SS). These parameters are in general extracted in compliance with the gradual channel approximation. By measuring the drain current (I_{DS}) with respect to gate voltage (V_G).

IV.5.2.2.1 Procedures

Electrical measurements were performed analyzer (Agilent 4156C). The transfer and output characteristics are measured.

1. Measuring I_D versus V_{DS} (Output Characteristics).
2. Set a certain value of voltage for V_{GS}.
3. Vary the voltage across drain (V_{DS}) from 0 to 1 V with steps of 10 mV and measure the corresponding drain current (I_D).
4. Repeat the procedure for different values of V_{GS}. (0V, 2V, 4V, 6V..... ,18V).
5. Plot the graph.
6. Measuring I_D versus V_{GS} (transfer characteristics).
7. Set a particular value of voltage for V_{DS} at 1 V. Start with a gate voltage V_{GS} of 0 V, and measure the corresponding drain current (I_D). Then increase V_{GS} in steps of 0.5 V until V_{GS} is 18 V. At each step record the drain current.
8. Plot the graph with I_D versus $V_{GS.}$
9. Calculate the transfer parameters from the graph.

IV.5.2.2.2 Results electrical characterization

The electrical characterization of ZnO thin-film transistors (TFTs) is crucial for understanding their device performance and optimizing their operation for specific applications. In this study, we conducted experimental measurements of the transfer characteristics of ZnO TFTs with HfO_2/Si and Al_2O_3/Si gate dielectric materials. By analyzing the ID (drain current) as a function of VGS (gate-source voltage), we can extract important device parameters and assess the overall performance of the TFTs.

The experimental transfer characteristics provide valuable insights into the behavior of the ZnO TFTs. By varying the V_{GS} while keeping other parameters such as V_{DS} (drain-source voltage) constant, we can observe how the drain current changes with respect to the gate voltage. This allows us to determine the threshold voltage, which is the gate voltage at which the TFT begins to conduct significant current. The threshold voltage is an important parameter that affects the switching behavior and overall performance of the TFT. Additionally, the experimental logarithmic transfer characteristics provide a logarithmic representation of the drain current as a function of the gate voltage. This logarithmic scale allows us to analyze the subthreshold region of the TFT, where the drain current is exponentially dependent on the gate

voltage. By analyzing the subthreshold region, we can extract the subthreshold swing, which represents the change in the gate voltage required to change the drain current by one decade. The subthreshold swing is a key parameter that characterizes the TFT's ability to control the flow of current in the low-power regime. Furthermore, by analyzing the experimental transfer characteristics, we can extract the effective mobility of the charge carriers in the ZnO TFT. The mobility represents the ability of the charge carriers to move through the channel region under the influence of the electric field. A higher mobility indicates better charge transport and faster device operation. Moreover, by analyzing the on-current and off-current values from the transfer characteristics, we can evaluate the TFT's performance in terms of its ability to provide high current when it is in the on-state and low current when it is in the off-state. This is crucial for achieving efficient device operation and minimizing power consumption.

In this study, we will present the experimental transfer characteristics and logarithmic transfer characteristics of ZnO TFTs with HfO_2/Si and Al_2O_3/Si gate dielectric materials. We will extract the threshold voltage, subthreshold swing, effective mobility, and assess the on-current and off-current performance of the TFTs. These results will provide valuable insights into the electrical characteristics of the ZnO TFTs and their potential for various electronic applications.

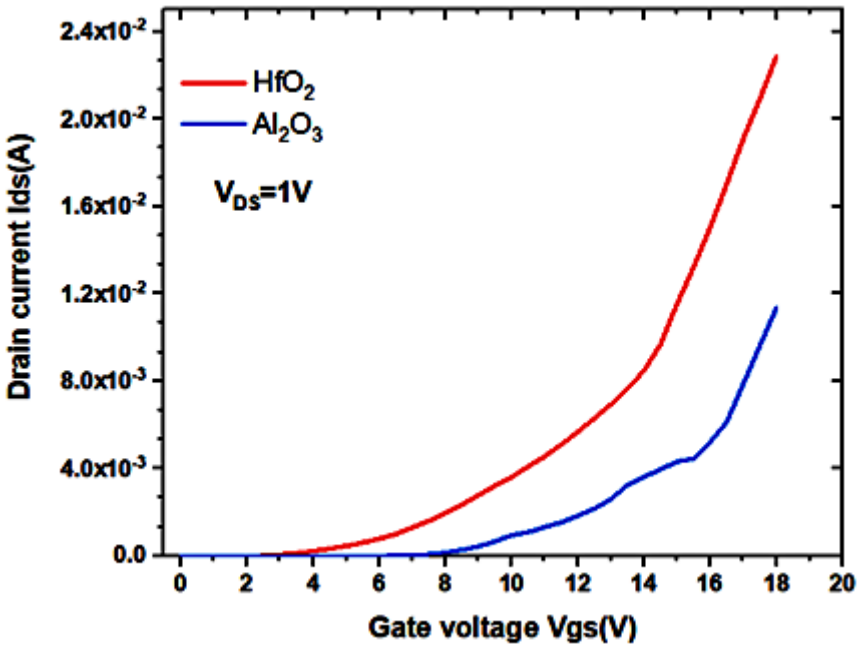


Figure IV-42:The experimental transfer characteristics $I_D=f(V_{GS})$ of the ZnO TFT (HfO_2/Si , Al_2O_3/Si).

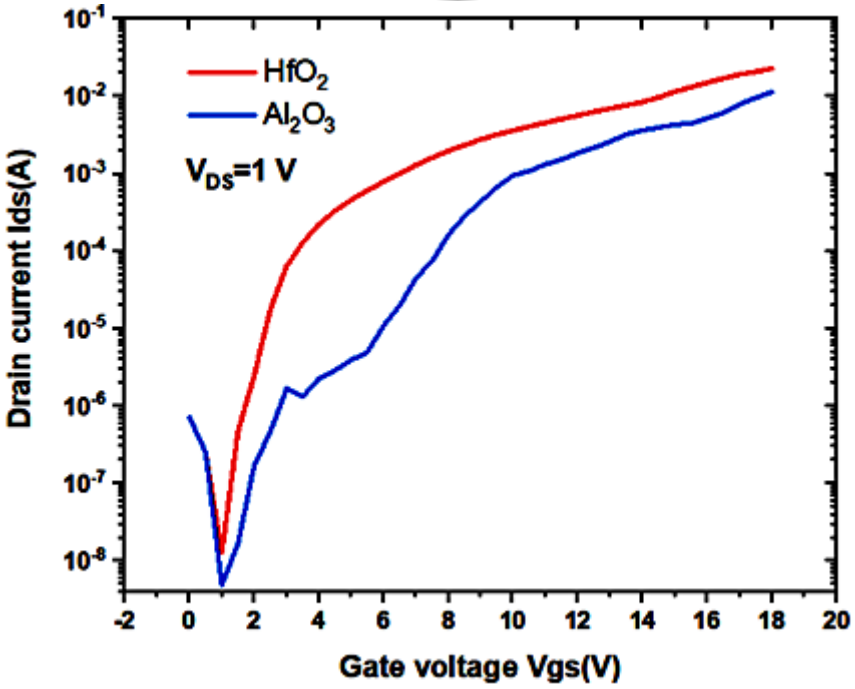


Figure IV-43:The experimental logarithmic transfer characteristics $I_D=f(V_{GS})$ of the ZnO TFT (HfO_2/Si , Al_2O_3/Si).

The fabrication of ZnO TFTs with HfO_2 and Al_2O_3 gate insulators involved depositing ZnO thin films on 100 nm-thick HfO_2 and Al_2O_3 gate insulators using a deposition technique, followed by the deposition of Al layers using DC deposition. This process results in the formation of a ZnO TFT structure with a gate insulator layer made of either HfO_2 or Al_2O_3, and a source, drain of Al. All put on silicon wafer in the form of a substrate. The resulting TFTs can be characterized and their electrical parameters can be extracted for analysis.

The methods of extraction parameters are explained in detail in the chapter II and parameters summary in the following Table IV-6.

Table IV-6:Summary the results extract of The (experimental logarithmic and experimental) transfer characteristics $I_D=f(V_{GS})$ of the ZnO TFT.

	Vth	**μeff**	**SS**	**Q**	**Ion**	**Ion/Ioff**
HfO_2	12	0.06	0.5	8.93×10^{16}	15.3×10^{3}	10^{5}
Al_2O_3	14.7	0.007	2	1.61×10^{17}	6.29×10^{3}	10^{5}

In summary, the fabrication of ZnO TFTs with HfO_2 and Al_2O_3 gate insulators involved depositing ZnO thin films on 100 nm-thick HfO_2 and Al_2O_3 gate insulators using DC deposition. The Al layers were also deposited using the same technique to serve as the gate electrode. The

extracted electrical parameters for the TFTs included Vth, SS and μeff which were found to be in the ranges of 12-14.7 V, 0.5-2 V/decade and 0.007-0.06 $m^2/(Vs)$, respectively. The value of Ion/Ioff is equal in both cases are 10^5.

Conclusion general

This thesis is an elaboration, characterization and simulation of thin film transistors based on Zinc Oxide. Four main parts were performed: the effect of temperature, deep defects, grain and boundary and fabricated ZnO-TFTs, and all this to observe the stability of the studied TFT.

The effect of temperature on the performance of ZnO thin film transistors (TFTs) was investigated in this study. The electrical characteristics and parameters of a polycrystalline zinc oxide (pc-ZnO) TFT were examined in relation to temperature. A comprehensive numerical simulation was conducted to understand the observed impact of temperature on the transfer characteristics of the pc-ZnO TFT. The drain current exhibited a significant dependence on temperature, with the activation energy decreasing linearly as the gate voltage increased. This indicated a strong dependence on the sub-threshold regime and a reduced dependence above the threshold voltage. The threshold voltage and electric field mobility, obtained from the current-voltage characteristics, also displayed temperature dependence. This behavior was attributed to the contribution of density of states (DOS) to channel conduction in the sub-threshold regime, whereas the DOS contribution was negligible beyond the threshold voltage. Furthermore, it was observed that the threshold voltage exhibited a proportional relationship with the electric field mobility. The simulated transfer characteristics of the pc-ZnO TFT demonstrated good agreement with the measured characteristics of pc-ZnO TFTs, validating the temperature dependence observed in the simulation.

The effect of illumination is important on the work and stability of ZnO TFT. A numerical simulation is carried using ATLAS to study the effect of illumination on low temperature because temperatures may be due to this dependence of the distribution functions of the nature of the incident light, defect created affected the transfer characteristics of a poly crystalline zinc oxide thin film transistor (pc ZnO TFT). The curve pre-illumination shows a three region it has a special point change with illumination. We study change drain current and gate voltage in terms of both mobility of electron free and donor-like tail states. Effect DOS at pc-ZnO TFT is great and affects mobility is weak. The most important result is that the effects μ_n on transfer characteristics of pc-ZnO TFT on the left sub-threshold slop curve pre-illumination means TFT shift to the accumulation state but impacted donor-like tail states on his right (depletion state). As for inverse defects holes and acceptor-like tail states there is no effect. Moreover, our research has two important fields in the domain of TFTs. The first is to

investigate the effect of light on the properties of TFTs. We know that this type of transistors is used a lot in optical applications; the second is theoretical, by set three points to the Logarithm curve transfer characteristics. We can see the contribution of pool-frank, and extract all the electrical properties of logarithmic transfer characteristics that are I_{on}, I_{off}, SS.

The objective of a separate investigation is to examine the influence of nano-grain size and grain boundaries on the performance of nanocrystalline zinc oxide (nc-ZnO) thin-film transistors (TFTs), with a specific focus on the deposition temperature. The deposition temperature is varied within a typical range of 80°C to 250°C to control the average size of the grains. The study involves the utilization of various techniques to analyze the structural characteristics of the grains and investigate the impact of grain size on the transfer characteristics of the TFT. This analysis primarily focuses on the relationship between drain current (I_D) and gate-source voltage (V_{GS}). Additionally, crucial parameters like the threshold voltage and subthreshold swing are extracted and examined to gain a deeper understanding of how the size of the nano-grains and their boundaries influence the electrical performance of nc-ZnO TFTs.

The fabrication of Zinc Oxide (ZnO) Thin Film Transistors (TFTs) with Hafnium Dioxide (HfO_2) and Aluminum Oxide (Al_2O_3) gate insulators involved several steps, including the deposition of ZnO thin films on 100 nm-thick HfO_2 and Al_2O_3 gate insulators. The deposition technique used in this process is called DC (Direct Current) deposition. This method involves applying a voltage between the target material (in this case, ZnO) and the substrate (HfO_2 or $Al2O_3$) in a vacuum chamber. As a result, the target material is sputtered off and deposited onto the substrate, forming a thin film. After the deposition of the ZnO thin film, Aluminum (Al) layers were deposited on top of the HfO_2 and Al_2O_3 gate insulators using the DC deposition technique. The Al layers were used as the gate electrode for the TFTs. To characterize the electrical properties of the ZnO TFTs, several parameters were extracted, including the threshold voltage (Vth) and the subthreshold swing (SS). Vth is the minimum voltage required to turn on the transistor, and SS is a measure of how steeply the transistor turns on and off. The Vth values for the ZnO TFTs with HfO_2 and Al_2O_3 gate insulators were found to be between 12-14.7 V. These values indicate that a relatively high voltage is required to turn on the TFTs. This may be due to the relatively thick gate insulator layer used in the fabrication process.

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